Switched-RC Radio Frequency N-Path Filters

Amir Ghaffari

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SWITCHED-RC RADIO FREQUENCY N-PATH FILTERS

DISSERTATION

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To My Family

Samenvatting

Afstembare filters zijn zeer gewenst voor mobiele radio communicatie en de wens bestaat deze op chip te realiseren samen met de overige benodigde zend- en ontvangst hardware. Vooral nu mobiele apparaten vele verschillende draadloze communicatie mogelijkheden dienen te ondersteunen (denk bv. aan GSM, Bluetooth, WiFi, UMTS) geïntegreerd op één chip, is er dringend behoefte aan afstembare filters. Ook groeit het mobiele internet gebruik enorm, zodat behoefte bestaat aan programmeerbare radio hardware die op een slimmere manier met het schaars beschikbare radio spectrum omgaat. Dit heeft geleid tot het concept van een "cognitieve radio", een stuk radio hardware dat op een intelligente manier dynamisch het spectrum gebruikt. Zo'n cognitieve radio vraagt om flexibel programmeerbare afstembare filters en meer algemeen "software defined radio" (SDR) hardware.

Het beperkte dynamische bereik van radio ontvangers vraagt om filtering van het radiosignaal direct bij de antenne. Dit filter dient de sterke ongewenste stoorsignalen te onderdrukken, die anders de radio ontvanger zodanig zouden oversturen dat door sterke vervorming betrouwbare draadloze communicatie onmogelijk wordt. Traditioneel wordt de filtering geïmplementeerd via aparte zgn. Surface Acoustic Wave (SAW) filters of Bulk Acoustic Wave (BAW) filters. Deze zijn echter relatief groot en duur vergeleken met een schakeling op een chip. Bovendien zijn ze voor een SDR grotendeels ongeschikt, daar ze een vaste (niet-afstembare) filter overdracht hebben. Op chip kunnen weliswaar LC filters gerealiseerd worden maar de kwaliteitsfactor Q van geïntegreerde spoelen is problematisch laag, terwijl "Q-enhancement" en "gm-C" filter technieken een te beperkt dynamisch bereik hebben. Er bestaat dus een duidelijke onderzoek uitdaging om tot integreerbare flexibel programmeerbare filters te komen met een groot dynamisch bereik.

In dit proefschrift worden zogenaamde "N-path" filters op basis van geschakelde RC circuits onderzocht. Deze filters gedragen zich als resonator voor frequenties rond hun schakelfrequentie, waarbij het mogelijk is zeer selectieve banddoorlaat of bandrejectie filters te maken. Het N-path filter concept past goed bij SDR omdat de filter frequentie digitaal te programmeren is via de schakelfrequentie, d.w.z. via een

digitale programmeerbare klokfrequentie. Omdat nieuwe CMOS technologieën meer capaciteit per oppervlakte kunnen bieden, terwijl MOS schakelaars een lagere weerstand met minder parasitaire capaciteit kunnen hebben, profiteren N-path filters van Moore's law.

Om de haalbaarheid van N-path filter voor SDR aan te tonen, is een 4-path differentieel switched RC banddoorlaat filter gerealiseerd, een 8-path single-ended filter en ook een differentieel bandstop (notch) filter, alle in 65nm CMOS technologie. Via mathematische analyse zijn de relevante filter overdrachten en ook diverse imperfecties geanalyseerd voor zowel N-path banddoorlaat en notch filters. Het geïmplementeerde banddoorlaat filter vertoont een gemeten $IIP3_{in\text{-}band}$>+14 dBm met een compressie punt $P_{1dB,in\text{-}band}$>0 dBm en een noise figure <6 dB. Het filter is afstembaar van 0.1-1 GHz. Voor het 8-path notch filter zijn de gemeten $IIP3_{in\text{-}band}$>+17 dBm, $P_{1dB,in\text{-}band}$>2 dBm, NF<3 dB, terwijl de notch frequentie afstembaar is van 0.1-1.2 GHz met een rejectie van >20 dB. Vooral het compressie punt en de IIP3 zijn veel hoger dan wat typisch met RF CMOS radio ontvangers mogelijk is.

De N-path filter techniek kan ook toegepast worden om spatiële filtering te realiseren. Dit is aangetoond door een 4-element phased-array bundelvormingssysteem te ontwerpen en realiseren. De 8-fase mixers transleren zowel de spatiële- als frequentie-domein filtering van basisband naar radio frequenties op de antenne ingang. Daardoor wordt een opvallend hoog compressie punt van tot wel +10 dBm gehaald voor signalen die buiten de band of antenne bundel vallen.

De N-path filter technieken die in dit proefschrift beschreven worden profiteren van CMOS schaling. Ze maken het mogelijk zeer lineaire afstembare filters te realiseren op een chip, en kunnen een sleuteltechnologie worden voor het realiseren van compacte flexibel programmeerbare radio ontvangst hardware.

Abstract

Tunable on-chip Radio Frequency (RF) filtering is highly desirable for cost effective wireless communication devices. As mobile wireless devices increasingly support multiple RF-bands, tunable RF filtering is wanted. The tremendous growth of wireless communication combined with scarcely available spectrum asks for new, more programmable radio hardware. This has led to the concept of a cognitive radio capable of smart dynamic spectrum access (DSA) which asks for software-defined radio (SDR) hardware, with flexibly programmable tunable filtering.

The limited dynamic range of a receiver front-end dictates the application of RF pre-filtering in front of the receiver, immediately at the antenna. This filter should reject strong out-of-band interfering signals that would otherwise block the receiver or would cause distortion components impeding reliable detection of a desired signal. Traditionally, discrete surface acoustic wave (SAW) or bulk acoustic wave (BAW) filters have been utilized as RF pre-filters. However, this adds to the size and cost of the total system. Even more problematic for cognitive radio, these filters are hardly tunable. State of the art on-chip LC filter techniques are typically limited by the low Q of spiral inductors or by the limited dynamic range in case of active Q-enhanced and gm-C filters. Hence, there is clearly an RF pre-filter research challenge.

In this thesis N-path switched-RC circuits are explored, aiming for RF pre-filtering for wireless transceivers. Around the switching frequency, these circuits can be modeled as a resonator and inductor-less high-Q band-pass or band-stop filtering is possible. The filter concept fits well to SDR as the center frequency is programmable by the switching frequency, i.e. via a digital clock. As new CMOS technologies provide higher density capacitors and MOS switches with low on-resistance and low parasitic capacitance, N-path filtering benefits from Moore's law.

To demonstrate feasibility, a 4-path differential switched-RC bandpass filter, an 8-path single-ended, as well as an 8-path differential bandstop (notch) filter have been implemented in 65nm CMOS technology. A mathematical analysis is presented to describe the filtering behavior as well as various imperfections for the N-path bandpass and notch filters. The implemented bandpass filter provides an in-band input referred third order intercept point $IIP3_{in\text{-}band}$>+14 dBm with compression point $P_{1dB,in\text{-}band}$>0 dBm at a noise figure NF<6 dB. The filter is tunable from 0.1-1 GHz.

For the 8-path notch filters, $IIP3_{in\text{-}band}$>17 dBm, $P_{1dB,in\text{-}band}$>2 dBm and NF<3 dB are achieved while the notch frequency is tunable from 0.1-1.2 GHz with the rejection of >20 dB. Especially the compression point and IIP3 are much higher than what is typically achieved with RF CMOS receivers.

The N-path filtering technique can also be applied for spatial filtering purposes. A 4-element phased-array system has been implemented in 65nm CMOS technology. 8-phase passive mixers translate the Spatial- and frequency-domain filtering from baseband to RF frequencies at the antenna inputs. As a result a remarkable input compression point P_{1dB} of up to +10 dBm is achieved for out-of-band/beam[1] blockers.

The N-path RF filtering techniques which are discussed in this thesis benefit from CMOS scaling. They present highly linear and tunable filters and pave the way to realize more compact and versatile RF transceivers.

[1] This includes two measurement cases: (1) In-beam and out-of-band (2) In-band and out-of-beam blockers.

Contents

Chapter 1

Introduction

1.1 Wireless Transceivers and Filtering

Wireless communication systems play a significant role in our daily life and many people recognize acronyms like GSM, WiFi/WLAN, Bluetooth and GPS. To fulfill the increasing demands for higher data rates and to cope with the plethora of existing and new applications, continuous innovations in wireless technology are wanted. Moreover, the tremendous growth of wireless communication combined with scarcely available spectrum asks for new, more programmable radio hardware. As will be discussed in section 1.2, this has led to the concept of a cognitive radio capable of smart Dynamic Spectrum Access (DSA). This asks for software-defined radio (SDR) hardware. In this thesis we will focus on programmable on-chip RF filtering for wireless applications. To understand the role of RF filtering, a typical zero-IF receiver and transmitter architecture which is suitable for CMOS integration is illustrated in Fig. 1.1. The received signal at the antenna is usually bandpass-filtered by an RF filter before applying it to a low noise amplifier (LNA). Typically this RF filter selects the band of desired signals, e.g. the GSM900 or GSM1800 band, or the Bluetooth 2.4 GHz band. The amplified signal at the output of the LNA is downconverted to baseband frequencies where it is lowpass filtered (LPF).

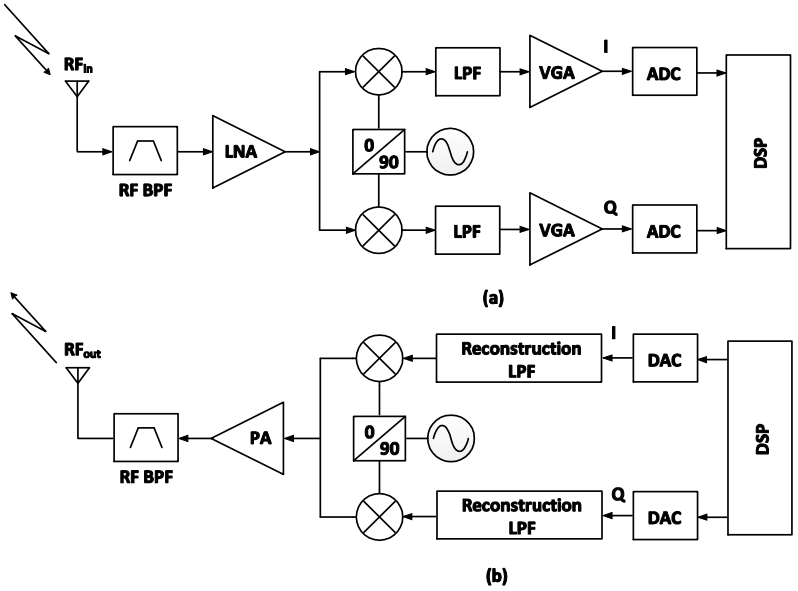

Figure 1.1. Zero-IF (a) Receiver (b) Transmitter architecture.

A variable gain amplifier (VGA) further amplifies the signal to fit to the dynamic range of the analog to digital converter (ADC). The rest of the processing is typically performed in the digital domain. Low-cost integration of tremendous amounts of digital signal processing (DSP) plays a crucial role in favoring CMOS IC-technology.

At the transmitter side the digital outputs are converted to an analog signal via a pair of Digital to Analog Converters (DAC). After filtering, frequency mixers upconvert the baseband signal to RF frequencies. A power amplifier (PA) amplifies the signal and after proper filtering to satisfy the transmission mask requirements the output signal is delivered to the antenna.

As indicated in Fig. 1.2, the received input signal at the antenna not only encompasses the desired channel to be received, but also interferers[1]. For in-band interferers obeying the same communication standard, e.g. a neighbor channel, the strength of the interference is limited, as defined by a radio standard. However, out-of-band blockers from other wireless networks may also exist, and can be much stronger (e.g. a TV transmitter delivering several kW).

[1] In this thesis we will apply "interfering" and "blocking" signals within the same meaning.

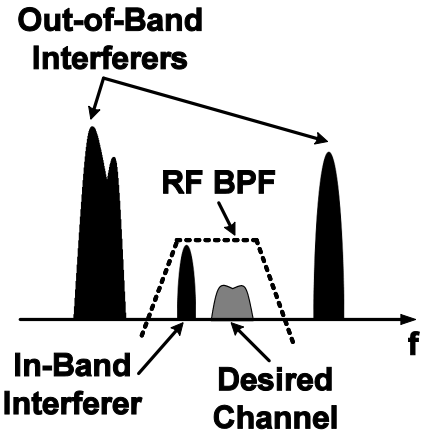

Figure 1.2. Typical received signal at the antenna.

If the interfering signals hit the LNA and other blocks in the receiver chain without proper filtering, the limited linearity and dynamic range of these blocks will deteriorate the signal to distortion ratio. If the intermodulation or cross-modulation distortion falls in the desired band, it degrades the sensitivity of the receiver, i.e. reliable reception is no longer guaranteed. In the case of high-power interferers the receiver might even be overloaded due to the limited compression point (P_{1dB}) of the receiver, which results in reduced amplification of the desired signal and consequently a further reduced signal to distortion ratio. To avoid these issues, the RF pre-filter should provide a proper rejection for out-of-band blockers without significantly affecting the in-band distortion level and noise figure (NF) of the receiver. Note that the insertion loss of the filter in the pass-band deteriorates the NF with the same amount.

RF filters based on surface acoustic wave (SAW) or bulk acoustic wave (BAW) resonators are widely used in wireless communications. These filters offer small feature size, high quality factor (Q), temperature stability and good power handling capability. However, they are mostly applied as off-chip components which adds to size and cost of the wireless devices. The thin-film nature of BAW filters and applying piezoelectric materials such as aluminum nitride, which is compatible with CMOS integration, provides a possibility to integrate these filters on top of the integrated RF transceiver to avoid external components [1]. However, this needs extra process steps compared to a conventional CMOS technology, which adds cost and yield issues. Moreover there are technological challenges such as limited

uniformity of piezoelectric layer which directly translates to the variation of the center frequency of the filter [2, 3].

In single standard traditional receivers it is quite common and also cost-effective to apply an external SAW/BAW filter to suppress out of band blockers. However in dynamic spectrum access (DSA) applications, where the desired received frequency band varies (e.g. 50 MHz-6 GHz) with location and time, a flexibly programmable RF filtering is wanted, and acoustic wave filters cannot offer this. Implementing a low-cost, on-chip tracking filter in this regard is strongly wanted for DSA applications.

In the following sections a brief introduction on DSA ideas is given. The aim is to illustrate the significance and necessity of the re-configurability of the RF pre-filtering in the up-coming generation of the wireless transceivers. Later on the possibilities of on-chip and off-chip tunable RF filtering will be discussed.

1.2 Tunable Filter Application Perspectives

1.2.1 Multi-Band Multi-Standard Transceivers

The tremendous growth of wireless communication systems in recent years resulted in many wireless standards. Nowadays a single handheld device might cover quad-band GSM-EDGE (850, 900, 1800, 1900 MHz) and W-CDMA/HSPA (850, 900, 1900, 2100 MHz) cellular networks. Moreover, a smartphone usually supports Wi-Fi connectivity at 2.4 and 5.8 GHz, and Bluetooth and GPS as well. Consideration of size, cost and battery lifetime have motivated the idea of sharing the hardware of the transceivers as much as possible in a single chip, leading to multi-band multi-standard transceivers. In order to receive multiple bands with a single RF front-end, a tunable filter or a bank of switchable filters is required. For a limited number of frequency bands a filter bank might be a practical option [4]. When increasing the number of frequency bands, the switchable filter bank concept increasingly becomes less practical. Tunable filtering is highly wanted in this regard.

1.2.2 Software Radio and Software-Defined Radio

Unlike digital signal processing circuitry in Fig. 1.1, the analog front-end hardware in many respects is not scaling favorably with new CMOS technologies.

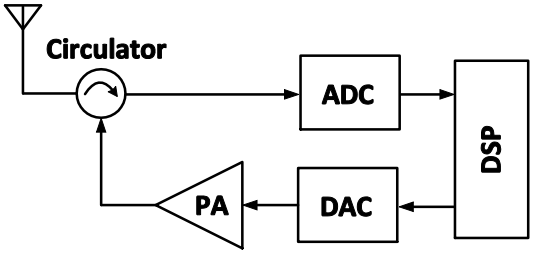

Figure 1.3. Software radio (SWR) architecture proposed by Mitola [5].

Even achieving the same linearity and dynamic range performance is problematic in newer technologies due to the reduced supply voltage and increased impact of short channel effects. Moreover, analog blocks at the receiver front-end are usually optimized for a specific application and adding flexibility and re-configurability to these blocks is difficult. These observations motivate attempts to minimize the amount of analog front-end hardware and push the digital part as close as possible to the antenna. The concept of a software radio (SWR) introduced by Mitola [5, 6] in the 90's, fits to this hardware trend. The SWR that Mitola envisioned is illustrated in Fig. 1.3.

In the architecture proposed by Mitola the received signal is directly digitized at RF by an RF ADC and fed to the DSP. At the transmitter the output of the RF DAC is amplified and transmitted via an antenna. The circulator routes the signals from the transmitter to the antenna and the received signals from antenna to the receiver without allowing the transmitted signals pass to the receiver. With the flexibility of the programming of the digital platform the SWR theoretically can receive any frequency band, with any modulation type and channel bandwidth. It might be even capable of receiving more than a single channel or wireless standard concurrently. The UK Defense Evaluation and Research Agency implemented a prototype of a SWR receiver for the 3-30 MHz HF band [7] in 2000. Still, the idea of SWR remains impractical so far for frequencies higher than UHF bands (30-300 MHz), especially due to the tough requirements on the ADC specifications. As high sample rate and high dynamic range is wanted simultaneously, power consumption estimates for an ADC covering the 1-6 GHz mobile bands can easily amount to about 1 kW [8]!

To reduce ADC requirements to what is feasible with state of the art CMOS ADCs, downconversion and filtering remains indispensable. The so-called Software-defined Radio (SDR) concept addresses this need, while still benefiting from digital flexibility. The SDR front-end architecture closely follows Fig. 1.1, but now with

sufficient bandwidth and/or re-configurability to receive RF signals in different frequency bands.

The RF pre-filtering which is required for SDR needs to be tunable to satisfy the multi-band reception property of a SDR. Although reconfigurable baseband filtering, for instance based on the switched-capacitor techniques discussed in [9], help to relax RF filter requirements, tunable RF pre-filtering is still required to suppress strong out-of-band blockers.

1.2.3 Cognitive Radio

In the traditional spectrum allocation regulations, almost all spectrum allocated for mobile radio communications, is regulated on a primary basis: dedicated to specific and exclusive use. However, this spectrum allocation is far from efficient, while there is a tremendously increasing demand for frequency spectrum. Although most parts of the spectrum below 6 GHz are allocated for specific use, spectrum measurement studies [10-12] show that most of the spectrum, in most of the places, most of the time remains unused. To increase efficiency, more liberal spectrum use has been advocated, based on knowledge of actual instantaneous local spectrum use. Such spectrum use is often referred to as Dynamic Spectrum Access or Opportunistic Spectrum Access. The term cognitive radio is also, loosely used, although dynamic spectrum access is just one possible aspect of cognitive radio as proposed in [13].

In this thesis we will use the term cognitive radio for a device with radio hardware and software, able to be aware of its operational environment so that it can dynamically and autonomously adjust its radio operating parameters. These parameters might include the modulation scheme, carrier frequency, bandwidth, transmitted power etc. The environment awareness might be provided by spectrum sensing [14, 15] available on-board and/or through geolocation database information. A comprehensive review of cognitive radio technology is presented in [16]. Similar to SDR, dynamic frequency band reception requires highly re-configurable RF pre-filtering.

Although cognitive radio is a general concept, recently research attention is mostly focused on the application of cognitive radio in TV bands. In the United States the Federal Communications Commission (FCC) proposed to construct new rulemaking in 2000, to offer possibilities for secondary spectrum use [17]. The idea is that secondary unlicensed (secondary) users will utilize the spectrum when it is

not used by users with a primary license. If a the licensed primary user starts communication, the secondary user should stop working or change its frequency band. In later reports [18-20] the FCC specified the regulations for fixed and portable devices operating in unlicensed TV white spaces (TVWS). Apart from mostly unused spectrum availability in VHF and UHF bands (54-698 MHz) which are applied for full service TV stations, this frequency range is also very suitable for wireless communication in terms of propagation characteristics such as path loss. Possible applications of TV white spaces include rural broadband access, new WiFi-like devices for increased broadband connectivity, machine-to-machine (M2M) applications and new mobile network operator deployments.

Utilization of TVWS frequency bands for cognitive radio applications also gained attention in term of international standardizations. For instance IEEE 802.22 [21] aims at wireless regional area networks (WRAN) providing broadband access in rural areas utilizing TV white spaces. IEEE 802.11af is another example aiming at Wi-Fi like networks also called White-Fi [22].

As dynamic spectrum access is first allowed for TVWS frequency bands, and as path loss is attractive in those bands, the filter designs proposed in this thesis are aiming at TVWS frequencies, aiming to cover the entire TV-spectrum.

1.3 RF Pre-Filtering for Dynamic Spectrum Access

As discussed earlier the desired band for DSA might vary over location and time. The interference caused by other licensed or unlicensed networks will then also vary, leading to variable distortion levels for different frequency bands [23]. RF pre-filtering is an indispensable requirement for reliable communication also for DSA. Consider a simple example where two single-tone interfering signals are generating intermodulation terms in the desired band due to nonlinearity of the front-end. If we assume the required IIP2 and IIP3 is such that the noise floor (N) of the receiver in the received channel is equal to the distortion level, then the required IIP3 and IIP2 for the front-end will be as following:

$$IIP3 = \frac{3}{2}P_{in} - \frac{1}{2}N \tag{1.1}$$

$$IIP2 = 2P_{in} - N \tag{1.2}$$

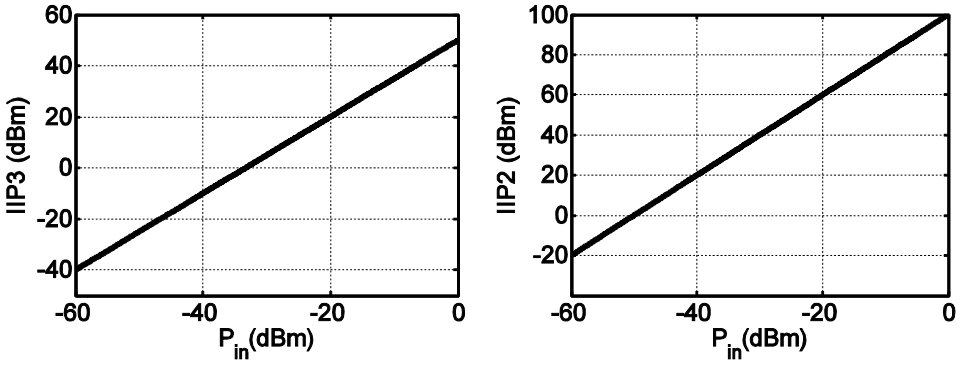

Figure 1.4. Required IIP2 and IIP3 for an RF front-end to bring IM2 and IM3 below a -100 dBm noise floor, assuming two blockers with each P_{in}.

In (1.1) and (1.2) all values are in dBm. Assuming 10 MHz channel bandwidth and 4 dB noise figure, a -100 dBm noise floor (N) results, and applying equations (1.1) and (1.2) the required IIP3 and IIP2 is illustrated in Fig. 1.4.

At the antenna, blocking signals up to 0 dBm are not unlikely, and the GSM and Bluetooth standards for instance specify blocker levels up to 0 dBm. Without pre-filtering, this would require an IIP3 of around 50 dBm and IIP2 of 100 dBm which are impractical to be achieved with the current CMOS technologies. Second order nonlinearity of the receiver front-end at RF frequencies produces sum and difference terms which might be removed by an octave bandwidth BPF [24]. Also, differential architectures for the receiver front-end building blocks can improve the even-order nonlinearity significantly. However, the odd higher order intermodulation terms and also the cross modulation from various interfering signals might fall in the desired band.

In a real situation more than just two blocking signals might hit the receiver front-end. In [25], 3rd order linearity requirements are derived in case of multiple tones or OFDM signals, considering both IM3 but also cross-modulation effects. Calculations for different scenarios show that often the amount of required linearity is not achievable with state of the art CMOS receivers without proper RF pre-filtering. Note that a filter would also have to satisfy such linearity requirements. Only if a filter can have better linearity and/or compression point than a receiver front-end, there is something to be gained. This is the aim of the current thesis.

It is not easy to quantify how much benefit DSA can bring, as it depends on many factors amongst which spectrum statistics. Marshall claims in an RFIC 2012

workshop that a factor of 10 improvement in aggregate communication throughput can practically be realized using DSA. He has shown that the use of tunable filters can significantly reduce the probability of receiver overload as well as the intermodulation induced noise floor in receivers, which can relax receiver IIP3 requirements easily by >20 dB [24, 26]. In an inspection based on a spectrum density mitigation algorithm called "Pick Quietest Band First" [24], it was shown that for a fixed receiver with IIP3 of -5 dBm and a pre-filter bandwidth of 20%, the non-cognitive radio has a 4 percent probability of overload, while the equivalent cognitive radio would have 10^{-7}. Moreover the statistical approach in [24] also illustrates that the most important resource to avoid front end overload in a cognitive radio is the filter. Increasing IIP3 also helps but is much less significant in reducing the probability that a given node will be overloaded.

1.4 RF Tunable Filtering Possibilities

Filters have a long history and countless options to realize filters exist. Here we mention somewhat arbitrarily a few options to realize tunable filtering. In [27, 28] tunable off-chip electromagnetic and cavity band-pass filters are discussed. These filters can have low insertion loss and remarkable out-of-band rejection with large power handling capabilities but their large size usually is not suitable for mobile handheld devices.

Electro-statically actuated MEMS resonators have also been proposed as CMOS compatible tunable bandpass filters [29, 30]. However, their high motional impedance level which might be at least several kOhms, limits their application in a 50 Ω environment at GHz frequencies, even though attempts are made to reduce this impedance [31]. With a high impedance level, power matching in 50 Ω systems will require LC matching networks which are usually narrow-band and to be avoided in the integrated circuits. Moreover, a high impedance level leads to large voltage swings that might cause significant distortion due to the nonlinearity of the electro-statistical resonators [32].

In acoustic wave filters (SAW/BAW) the resonance frequency is defined by the piezoelectric material dimensions and its properties. Currently the piezoelectric effect is not strong enough to change the center frequency significantly.

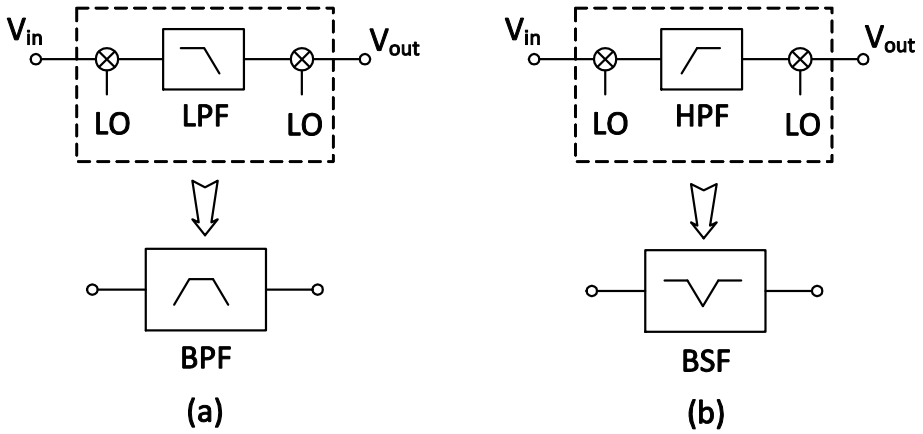

Figure 1.5. Frequency translated filtering (a) a lowpass filter is translated into a bandpass filter (b) a highpass filter is translated into a bandstop or notch filter.

For instance for BAW filters typically the frequency change is less than 20 ppm/V [33] which means 0.2% variation at the resonance frequency even if we apply a DC voltage of 100V. There is an active research community proposing new materials and implementation techniques, however widely tunable acoustic wave filters are not yet available [34]. There have also been efforts to implement tunable filters with fixed resonators (e.g. BAW/SAW) and tunable capacitors [35]. The tuning range of these filters is very small and usually these techniques are used to compensate the variations of the center frequency posed by the process [36].

In this thesis we are looking for tunable on-chip filtering solutions. On-chip LC filters with variable capacitors are usually suffering from losses of on-chip inductors. Q-Enhancing techniques apply on chip low Q inductors in combination with an active negative impedance to compensate for resistive losses in the inductors. These filters have a limited dynamic range restricting their usefulness as RF pre-filters. RF active filters provide high Q and tunability. However, the linearity and noise of these filters are not good enough to be used as RF pre-filtering block after the antenna [37, 38].

To implement on-chip RF pre-filtering, a technique referred to as frequency-translated filtering is gaining strong interest in recent years. The concept is illustrated in Fig. 1.5. The input signal at RF frequencies is downconverted before applying it to a lowpass or highpass filter (LPF/HPF). The filter output signals are upconverted again to RF. Overall, a bandpass or bandstop filter at RF frequencies is emulated. The baseband filters might be as simple as an RC network and frequency

mixers can be implemented with hard driven CMOS switches. As the bandwidth of the baseband filter can be much lower than the RF center frequency (=switching frequency), the resulting Q of the RF bandpass filter can be high. As an example, a 5 MHz baseband frequency and a 1 GHz switching frequency would result in a Q of 100, which is an order of magnitude higher than feasible with CMOS LC-filters. Moreover the center frequency is digitally tunable with the clock frequency.

The architecture shown in Fig. 1.5 is usually not implemented with one mixer-filter-mixer signal-path, but usually with multiple paths, driven by multiphase clocks. This is the reason that these kind of filters are also addressed as "N-Path filters" in literature. Although the concept of filtering based on passive mixers was developed bottom-up during research in the IC Design Group, we discovered later that the idea has much older roots. A brief history of the N-path filtering is discussed in the next section.

1.5 Frequency Translated N-Path Filtering

N-path filtering in the electronic domain received considerable attention in the 60's [39, 40] as a continuous-time filtering technique at kHz-range frequencies. There is even older work on electro-mechanical implementations, in which a mechanical motor drives rotating switches to implement the multi-phase clocking, with RC filters to realize the baseband filter (the term "commutating filters" is sometimes also used).

Fig. 1.6 shows two cascaded 4-path filtering stages which are used to realize a bandpass filter at 108 kHz center frequency [40]. The switches are implemented by solid state diodes and capacitors with off-the-shelf components. In chapter 2, detailed analysis will show that the switches in Fig 1.6 are in fact realizing a multiphase passive mixer which translates the lowpass characteristic of the RC network to create a bandpass behavior around the switching frequency.

Later there have been attempts to apply N-path networks to implement higher order filtering. In [41], two 3-path RC resonators have been replaced in an active RC lowpass filter to realize a bandpass filter with two complex pairs of poles. In [42], the LC resonators in a coupled resonator LC bandpass filter prototype for a center frequency of 5.8 kHz are replaced by N-path switched-RC networks to implement a higher order N-path bandpass filter.

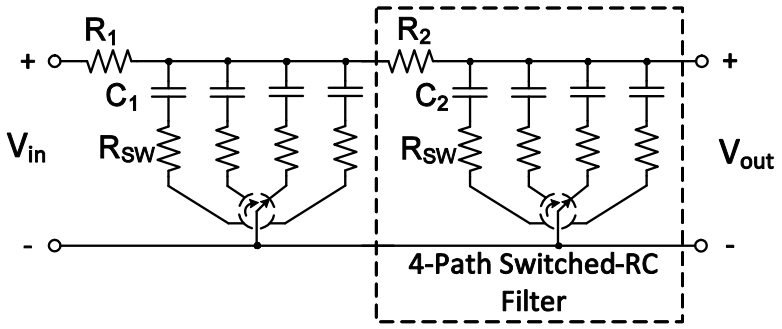

Figure 1.6. Two stage cascaded 4-path filter [40].

N-path filters have been applied with gyrators as well. In an LC low pass filter prototype the inductor might be replaced by a gyrator and capacitor. If the capacitors are replaced by N-path switched-RC networks then the lowpass characteristic can be transferred to a bandpass one [43].

The N-path filters discussed so far are time-variant circuits that produce a continuous-time output. In the 80s, the N-path technique has also been adopted in discrete-time switched-capacitor filters [44-46]. Instead of simple switched RC networks in each path, more complex blocks including operational amplifiers have been applied to realize higher order switched-capacitor N-path filters. The mismatch between different paths can deteriorate the filter functionality. To mitigate path mismatch effects, Fettweis and Wupper introduced the concept of pseudo-N-path filters [47]. In these filters there is actually only one physical path in which the sampled data is transferred to different capacitors via an analog shift register. Another problem of N-path filters is the frequency selectivity around the harmonics of the switching frequency. In [48] a passive approach with just switches and capacitors is presented to suppress harmonic selectivity at the even harmonics of a single-ended N-path filter. Normally the even harmonics might be rejected via a differential architecture. To increase the filter order avoiding the active components, an all passive switched-capacitor discrete-time domain approach is developed in [44] in which just capacitors and switches are applied.

In recent years continuous-time frequency-translated filtering has been explored in different forms to realize RF filtering in receiver. Some examples are shown in Fig. 1.7. In [49] a frequency-translated notch filter is applied in the lower feedforward path of Fig. 1.7.a, and its output signal is subtracted from the output of the main amplifier path. Overall, this realizes a bandpass filter around the mixing frequency at the output of the gain block.

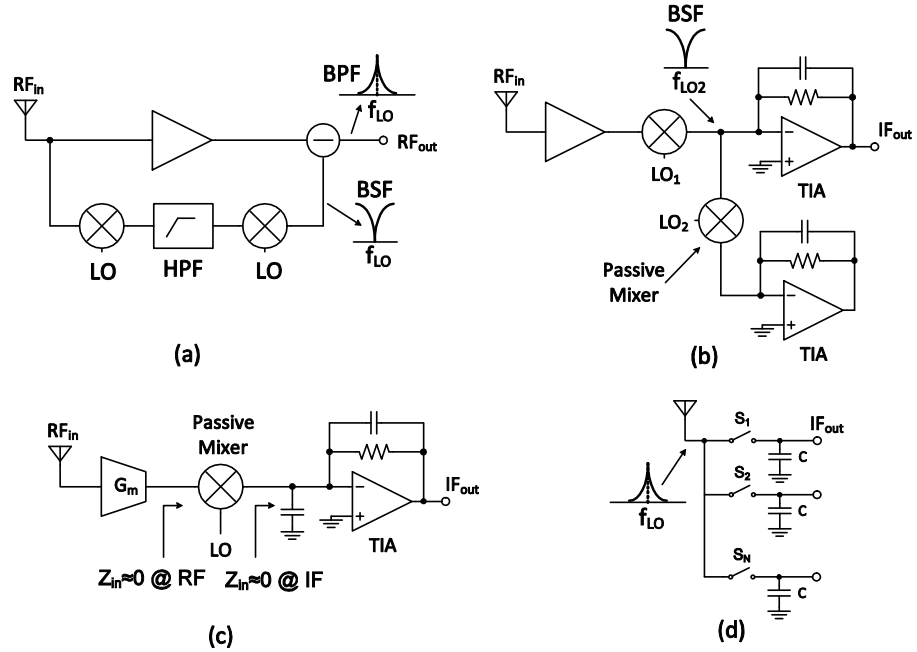

Figure 1.7. Frequency translated filtering (a) Translational loop [49]. (b) BSF or notch filter at IF frequencies [50]. (c) Highly linear receiver [51]. (d) Mixer first receiver [52], [53], [54].

Another example of frequency translated filtering is shown in Fig. 1.7.b, where the virtual ground impedance of a Trans-Impedance Amplifier (TIA) at baseband is transferred around f_{LO2}. As the virtual ground impedance increases with baseband frequency, overall a notch filter results that can suppress blockers [50].

Another way to exploit the low virtual ground impedance is shown in Fig. 1.7.c [51]. Here, the low input impedance of the TIA is transferred around the LO frequency by a passive mixer to limit the voltage swing at the output of the input transconductance (G_m) block. In this way voltage gain at RF is low which is beneficial for linearity in general [55], but even more for nanometer CMOS devices in which large drain voltage swings strongly degrade linearity [51]. Note that, in contrast to Fig. 1.7.b, a wideband low virtual ground impedance is required, which is one of the reasons why a shunt capacitor to ground is added at the virtual ground node. A different class of receivers completely omits an LNA and directly put the mixer at the antenna [52-54]. An example of such a "mixer-first" receivers is shown in Fig. 1.7.d with a capacitive termination [54].

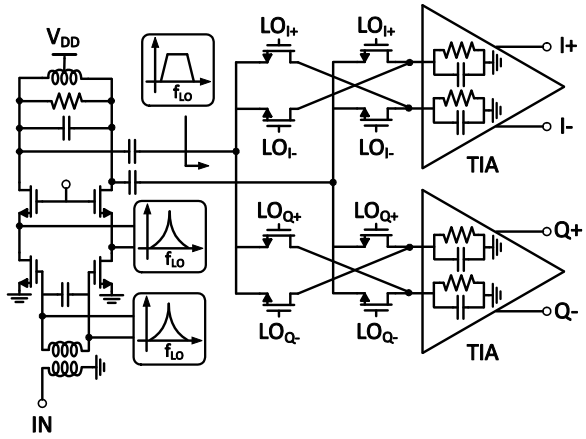

Figure 1.8. Application of N-path filtering in the receiver front-end [56].

If we consider the antenna as a source with resistance, this circuit actually is the switched-RC N-path bandpass filter used in Fig. 1.6, if the output is taken at the antenna node. Instead of a capacitor only, often also a TIA with RC load is used [53], which allows for realizing impedance matching. In recent years and especially during the period of the research project which led to this thesis some applications of the switched-RC N-path filters were presented in literature [57-59]. For instance as indicated in Fig. 1.8, two 4-path switched-RC filters are connected to the gate and drain of the input NMOS transistors providing bandpass filtering around f_{LO}. Moreover the RC-filtering at the input of TIA is also upconverted to RF frequencies via passive mixers realizing bandpass filtering at the output of LNA. In [58] N-path filters are applied to provide image rejection in a super-heterodyne receiver.

As mentioned earlier the zero-IF voltage outputs on the baseband capacitors shown in Fig. 1.7.d undergo a frequency filter similar to the RF node before the switches and even better because switch resistance doesn't limit achievable filter attenuation. Then the question may arise, what is the benefit of applying RF node filtering instead of exploiting the readily available baseband signals? We found the following benefits:

1. Compared to receivers starting with an LNA or Low Noise Trans-Conductance Amplifier (LNTA), out-of-band linearity and compression point can be significantly higher, making it sensible to use an N-path filter in front of such receivers.
2. With the application of N-path filters in front of LNA or even embedded in LNA as Broadcom proposed in [56] (see Fig. 1.8), compared to other mixer-

first receivers, the linearity becomes similar, but 1/f noise is better. This is because typically voltage gain is required at RF before downconversion, to reduce the Flicker noise of IF amplifiers sufficiently. Note that a mixer-first I/Q architecture requires 4 baseband low-noise amplifiers at baseband with low 1/f noise, while one LNA without 1/f noise requirements suffices at RF. This typically renders a significant power dissipation advantage.

1.6 Research Objectives

This thesis focusses on N-path filters for RF frequencies. Most traditional analog building blocks suffer from the lower supply voltage headroom and short-channel effects of downscaled CMOS technologies. However in new CMOS technologies, MOS switches with low on-resistance and with less parasitic capacitances are available. Also capacitors with high quality factors can be realized, exploiting the many metal layers. Some processes even have high density capacitor realized via a thin oxide between two metal layers (so called "MIM capacitors"). These passive components are very linear and can hence be an attractive basis for high linearity programmable filters to improve the performance of receiver front-ends in new CMOS technologies.

The N-path filtering concept provides high-Q filtering with just switches and capacitors without any inductors. Despite of the fact that the N-path filters were well known in the 60s, their application to RF frequencies has not been considered until recently. This thesis aims to show that such filters can have excellent tunability, high linearity and compression point and low noise in modern CMOS technologies. We will aim at tunable high-Q filters for DSA applications in the TV bands. In this thesis we are aiming to provide closed form equations to model N-path switched-RC filters and demonstrate these filters through CMOS prototypes. Both N-path bandpass and bandstop (notch) filters will be discussed. Moreover the N-path filtering will be applied to provide spatial filtering in a 4-element phased-array system.

The switched-RC N-path filters are in fact Linear Periodically Time Variant (LPTV) systems. Since the 60's several analysis methods have been developed based on the time-varying transfer function introduced by Zadeh [60] for N-path filters in the context of LPTV systems. An approximate analysis just for the main side band of N-path filters in the form of commutated capacitors as seen in Fig. 1.6 was presented in [39]. More accurate analysis approaches are presented in [61, 62]. However none

of these works properly describe the frequency aliasing issues associated with N-path filters.

More recently, analysis results have also been presented by Andrews [63] and Mirzaei [64]. In their approximate approaches the RF impedance seen by the N-path filter might include also reactive components. However, the analysis presented here is more comprehensive for the switched-RC case, covering all frequencies and mixing side-bands. Moreover, unlike previous works the equations are valid for all RC values. In this thesis we will assume that the RF impedance seen by the N-path network is purely resistive. Thus the general form of state-space analysis for LPTV networks presented in [65], leads to a single state one for the networks we are considering in this thesis [66]. One set of closed form equations for switched-RC N-path filters will be derived. Then the analysis results will be applied to describe filter properties including possible imperfections such as noise and harmonic mixing.

Here we will mostly work on the N-path filters in the context of a receiver. N-path filtering might also proof beneficial for transmitters or frequency synthesizers. Then the harmonic mixing and limited power handling might probably be limiting factors.

Most parts of this thesis are published in [67-71]. It is worth noting that some relevant aspects are not discussed in our work, partly because they are already addressed by other publications. For instance the phase noise and switch nonlinearity effect which is not discussed here, is covered in [64].

1.7 Thesis Organization

The organization of this thesis is as follows:

In chapter 2, an architecture for switched-RC differential N-path bandpass filters is discussed. An intuitive understanding of the operation of this N-path filter architecture leading to a mathematical modeling and exact analysis of the circuit is presented. Measurement of an implemented prototype of a differential 4-path filter in 65 nm CMOS technology is provided and compared with state of the art. The derived equations describing the properties of the N-path filters are in a general form, however the numerical examples are presented for the 4-path circuit implemented on-chip. An RLC tank circuit which provides a simple model around the switching frequency is derived for the N-path switched-RC networks.

In chapter 3, N-path notch filters are presented. Here both single ended and differential architectures are discussed. Just as for the N-path bandpass filters, a set

of closed-form equations describing the input-output desired and undesired transfers are derived. Moreover notch filters are also modeled as a simplified parallel RLC tank circuit around the notch frequency.

In chapter 4, the N-path technique is applied to implement a 4-element phased-array system. The Spatial- and frequency domain filtering is provided at the antenna inputs. This brings interference rejection for out-of-band/beam blockers already at the antenna inputs. A prototype is implemented and measurement results are compared with state of the art work presented in recent years.

Chapter 5 concludes the thesis, providing a summary of the key parameters of the implemented chips and general insights for the N-path filters and phased-array system discussed in preceding chapters.

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Chapter 2

Tunable High-Q N-Path Bandpass Filters: Modeling and Verification[1]

2.1 Introduction

Inductor-less tunable filters based on periodically time variant networks have been addressed in literature under different names such as N-path filters, sampled data filters, commutated capacitors, etc. [1-7]. Discrete-time switched capacitor N-path filters are probably best known [4], but here we focus on their continuous-time predecessors. Fig. 2.1 shows a block diagram of an N-path filter composed of N identical Linear Time-Invariant (LTI) networks with impulse response h(t) and 2N frequency mixers (or modulators), driven by time/phase shifted versions of the clock p(t) and q(t). The time shift between two successive paths is T/N, where T is the period of the mixer clock. If the LTI networks exhibit a lowpass characteristic around DC, the mixing results in a band-pass around the mixing frequency.

[1] This chapter has been published in the IEEE Journal of Solid-State Circuits:
A. Ghaffari, E. A. M. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable High-Q N-Path Band-Pass Filters: Modeling and Verification," Solid-State Circuits, IEEE Journal of, vol. 46, pp. 998-1010, May 2011.

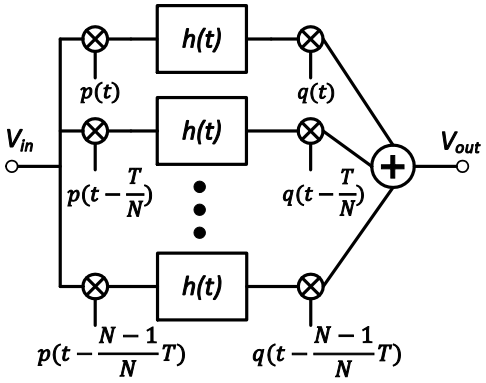

Figure 2.1. Architecture of an N-path filter [1] (p and q are the mixing functions and T is the period of the mixing frequency).

Simply put, the input signal is down-converted to baseband, filtered by the LTI network and then up-converted again to the original band of V_{in}. The center frequency is determined by the mixing frequency, insensitive to filter component values. A high mixing frequency combined with a narrow low-pass filter bandwidth allows for a very high filter-Q.

While time-continuous N-path filters have been proposed for kHz operating frequencies in the 60's [2], they seem to have been largely forgotten until recently. CMOS technology now allows N-path filters to work at TV-band RF frequencies [5, 6] and even above 1 GHz [7]. In [5] an 8-path single-ended structure is used, and in [6] we proposed a differential 4-path filter combined with a broadband off-chip transformer. In [7] the differential 4-path filters are applied in a quad-band SAW-less receiver. This chapter aims to model and verify N-path filter performance.

Using Linear Periodically Time-Variant (LPTV) analysis, exact expressions for the frequency response of differential N-path filters are derived. In [3] state-space analysis was used to derive the steady-state and transient response for a single-ended N-path filter, which is however not directly applicable to our differential architecture. We will derive one set of equations that characterizes filtering but also possible imperfections like harmonic folding, noise and the effects of the clock phase imbalance and mismatch. Moreover, an equivalent RLC tank circuit will be derived to approximate N-path filter behavior around the center frequency. Finally, we will verify the model via extended experimental results compared to [6].

In section 2.2 we will derive the differential N-path filter architecture starting from Fig. 2.1 and then analyze its transfer function in section 2.3. Section 2.4

presents basic characteristics of the differential N-path filter. Its chip implementation is discussed in section 2.5 and section 2.6 covers the measurement and verification versus the model.

2.2 N-Path Bandpass Filter Concept

We will now derive the differential N-path filter from Fig. 2.1, where we aim for a high-linearity implementation using MOS switches as passive mixers, and RC lowpass filters (see Fig. 2.2.a). Furthermore we will try to develop some intuitive understanding of the filter behavior.

2.2.1 Single-Ended Switched-RC N-Path Filter

Fig. 2.2.c shows a multiphase clocking scheme for the switches with non-overlapping on-times. Thus no charge exchange between capacitors can occur. For this reason and since a resistor is a memory-less element, it can be shared by all paths and shifted in front of them (Fig. 2.2.b). Moreover, if the clocks for the first and second set of switches are identical, the first set can also implement the function of the second set. V_{out} becomes then available between the shared resistor and switches.

Fig. 2.2.b shows the resulting single-port single-ended N-path filter (V_{out} is both input and output port). If we would use the capacitor voltages as outputs, the circuit behaves as a highly linear multiphase passive mixer [8, 9]. To intuitively understand the filter behavior of Fig. 2.2.b it is useful to model it as a two-step process: 1) the input signal experiences downconversion and lowpass filtering passing through the switches to the capacitors; 2) the same switches upconvert the filtered capacitor voltages to the output node. Another way to understand the filtering is to realize that at any moment one and only one capacitor is connected to the output node. If we assume that the time constant $RC>>T_s/N$, the output voltage will be the average of the input voltage V_{in} over the time that the capacitor "looks at V_{in}". If the frequency of V_{in} is equal to the switching frequency, a particular capacitor will periodically observe the same part of the input waveform during every period. As each capacitor sees another part, the result is a staircase approximation of V_{in}, see Fig. 2.2.d (4-path example). In fact, the capacitors experience a steady DC voltage and, in first order approximation, conduct no current. If the input frequency deviates from the clock frequency the signal portion seen by a capacitor will "travel over the period" and the capacitors experience an AC voltage (with $f = \Delta f$).

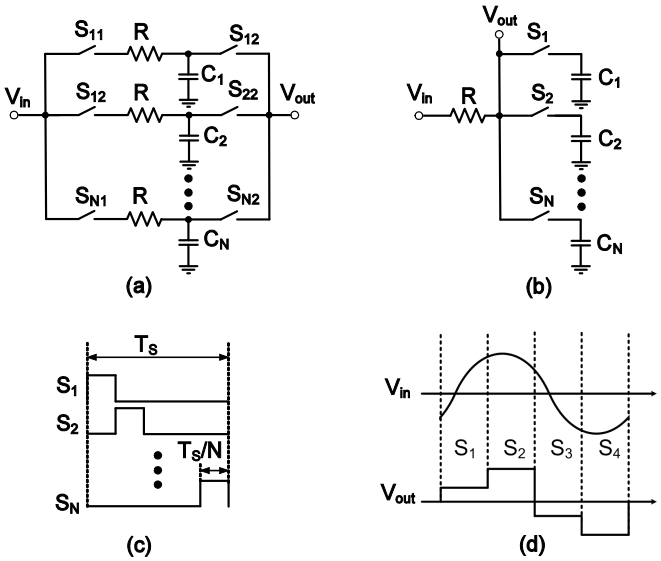

Figure 2.2. (a) Switched-RC N-path filter. (b) Single-port, single-ended N-path filter. (c) Multiphase clocking. (d) Typical (in-band) input and output signal.

Thus the capacitors conduct current while switches are "on" and the average voltages on the capacitors become closer to zero. Consequently signals at input frequencies below or above the switching frequency will be suppressed with an amount depending on the offset from the switching frequency, on-time of the switch and RC time.

2.2.2 Differential Switched-RC N-Path Filter

If we repeat the analysis for input signals around the harmonics of the clock frequency, we also find non-zero average values. This fits to the comb-like characteristic of N-path filters [1], i.e. its repetitive selectivity around harmonics of the switching frequency. The differential architecture of Fig. 2.3 aims to cancel the even harmonic responses. Each path is differential-in and differential-out, but contains one grounded capacitor connected to two anti-phase driven switches. A 4-phase 25%-duty-cycle clock provides all required clocks (see Fig. 2.3). Now, for input signals around the even harmonics of the clock frequency, no net charge is stored on the capacitors in steady state and no upconverted signal appears at the output.

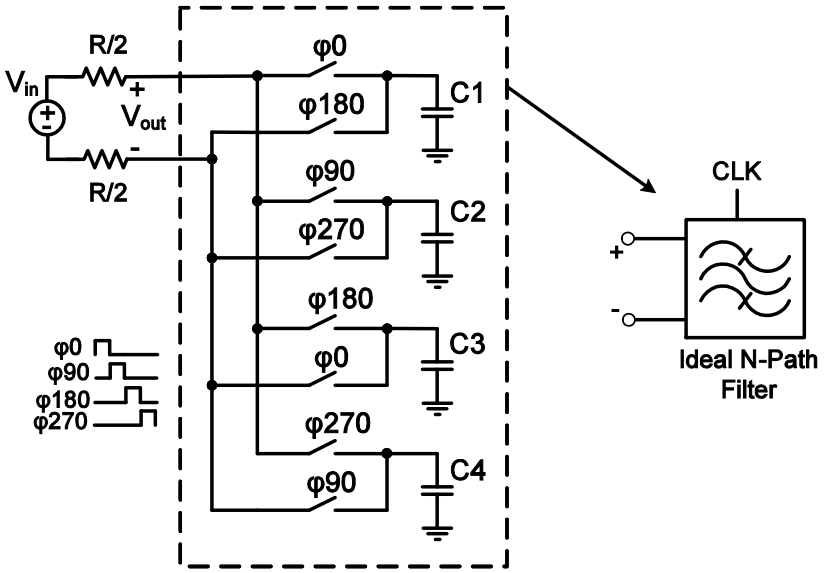

Figure 2.3. Single port differential 4-path filter.

2.3 Analysis

To model the behavior of the N-path filter quantitatively, we will now apply LPTV state-space analysis [10, 11] to derive the exact shape of the transfer function of a differential N-path filter.

2.3.1 State-Space Analysis of LPTV circuits

For an LPTV network which is periodic with the frequency $f_S = 1/T_S$, the output spectrum is related to the input spectrum as [12]:

$$Y(f) = \sum_{-\infty}^{\infty} H_n(f) U(f - nf_S), \tag{2.1}$$

where $U(f - nf_S)$ represents the shifted version of the input spectrum to account for frequency translation (mixing), while $H_n(f)$ describes the spectral shaping (filtering) properties of an LPTV network. To simplify analysis, we make two assumptions: (1) The switches are ideal, i.e. their off-impedance is infinite and on-impedance is zero; (2) Switching occurs instantaneously.

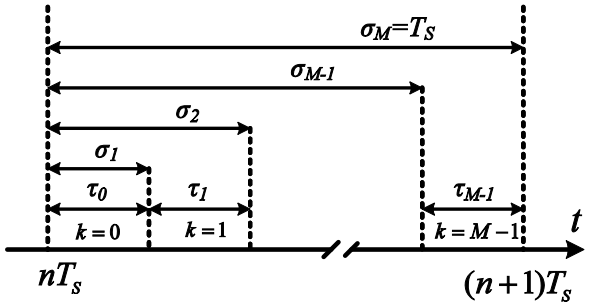

Figure 2.4. Time intervals for the state-space analysis.

The time interval $nT_s < t < nT_s + T_s$ is divided into M portions (M is the number of the states) and each portion identified by k can be represented as $nT_s + \sigma_k < t < nT_s + \sigma_{k+1}$, k=0,…, M-1 and $\sigma_0 = 0$ (see Fig. 2.4). During each interval there is no change in the state of the switches and the network turns to an LTI system. The state equations for interval "k" can be written as:

$$\begin{aligned} \dot{x}_k(t) &= A_k x_k(t) + B_k u(t), \\ y(t) &= C_k x_k(t) + D_k u(t), \end{aligned} \tag{2.2}$$

where $u(t)$ is the input vector, $x_k(t)$ the state vector and $y(t)$ the output vector. If we define $u_k(t)$ and $y_k(t)$ to be equal to the input $u(t)$ and output $y(t)$ respectively during the k[th] interval, and zero otherwise, the state equations in (2.2) can be reformulated as [10, 11]:

$$\begin{aligned} \dot{x}_k(t) &= A_k x_k(t) + B_k u_k(t) \\ &\quad + \sum_{n=-\infty}^{\infty} (x_k(nT_S + \sigma_k)\delta(t - nT_s - \sigma_k) - x_k(nT_s + \sigma_{k+1})\delta(t - nT_s - \sigma_{k+1})), \\ y_k(t) &= C_k x_k(t) + D_k u_k(t). \end{aligned} \tag{2.3}$$

In (2.3) the Dirac's delta function $\delta(t)$ has been used to add the effects of the initial conditions to the equations at the beginning of an interval, while subtracting it at the end of the interval. Then the output $y(t)$ is the sum of all responses from M states in the system:

$$y(t) = \sum_{k=0}^{M-1} y_k(t). \tag{2.4}$$

Since we are interested in the spectrum of the output of the system we need to take the Fourier transform from (2.4). It can be shown [11] that if we apply a complex exponential $u(t) = Ae^{j2\pi ft}$ as input, the output state at discrete moments can be calculated by reforming the state equations to a set of difference equations at the switching moments. Consequently the relation between the input and the output will be of the form:

$$x_k(nT_s + \sigma_k)\delta(t - nT_s - \sigma_k) = G_k(f)Ae^{j2\pi ft}\delta(t - nT_s - \sigma_k). \tag{2.5}$$

The input spectrum can be represented as a summation of sinusoidal signals. As a result the infinite summation in (2.3) takes the form:

$$\begin{aligned}\sum_{n=-\infty}^{\infty}(x_k(nT_s + \sigma_k)\delta(t - nT_s - \sigma_k) - x_k(nT_s + \sigma_{k+1})\delta(t - nT_s - \sigma_{k+1})) = \\ \left(\sum_{n=-\infty}^{\infty}(G_k(f)\delta(t - nT_s - \sigma_k) - G_{k+1}(f)\delta(t - nT_s - \sigma_{k+1}))\right)u(t).\end{aligned} \tag{2.6}$$

By applying (2.6) to (2.3) and taking the Fourier transform, the spectrum of the state vector becomes:

$$\begin{aligned}X_k(f) &= \sum_{n=-\infty}^{\infty}H_{n,k}(f)U(f - nf_s), \\ H_{n,k}(f) &= (j2\pi fI - A_k)^{-1} \times \begin{pmatrix} B_k\dfrac{1 - e^{-j2\pi nf_s\tau_k}}{j2\pi n}e^{-j2\pi nf_s\sigma_k} + f_sG_k(f - nf_s)e^{-j2\pi nf_s\sigma_k} \\ -f_sG_{k+1}(f - nf_s)e^{-j2\pi nf_s\sigma_{k+1}} \end{pmatrix},\end{aligned} \tag{2.7}$$

where τ_k is the length of kth time interval (see Fig. 2.4) and I is an identity matrix.

2.3.2 Analysis of the Differential Single-Port N-path Filter

We will apply the analysis procedure described in the previous part to derive the output spectrum of the differential N-path filter. Although Fig. 2.3 illustrates a 4-path architecture, analysis is done for a general differential N-path system. At any moment two capacitors are connected to the differential output through two switches, which are activated with the same phase of the input clock.

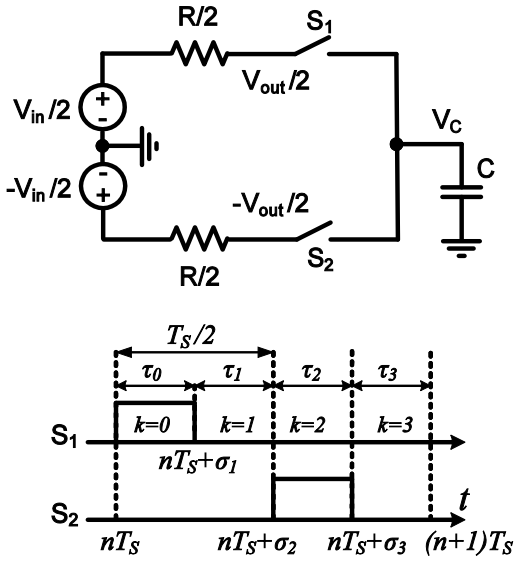

Figure 2.5. Differential Single-path circuit and the clock phases for the switches.

The resulting time-domain output signal is the superposition of the signals from different capacitors at different moments without any overlap. Since there is no interaction between capacitor voltages, the analysis of the simple network illustrated in Fig. 2.5 suffices, where just one path is illustrated with its timing diagram for the switches. The state equations for this circuit are:

$$\begin{aligned}
&\dot{v}_c(t) = -\frac{2}{RC}v_c(t) + \frac{1}{RC}v_{in}(t) && nT_s < t < nT_s + \sigma_1, \\
&v_c(t) = v_c(nT_s + \sigma_1) && nT_s + \sigma_1 < t < nT_s + \sigma_2, \\
&\dot{v}_c(t) = -\frac{2}{RC}v_c(t) - \frac{1}{RC}v_{in}(t) && nT_s + \sigma_2 < t < nT_s + \sigma_3, \\
&v_c(t) = v_c(nT_s + \sigma_3) && nT_s + \sigma_3 < t < (n+1)T_s,
\end{aligned} \tag{2.8}$$

where $v_c(t)$ is the voltage on the capacitor in Fig. 2.5. If one of the two switches is on, the output voltage will track the voltage on the capacitor. When switches are off, the voltage on the capacitor will be held, but will not affect the output. Hence, the output spectrum contribution will be calculated in the track-mode.

As the capacitor will deliver either $V_{out}/2$ (S_1 on) or $-V_{out}/2$ (S_2 on), this contribution is $v_{out}(t) = 2v_c(t)$.

As a result, A_k and B_k in (2.7) should be defined from either the first or third equation in (2.8), depending on which switch is on. As a result, according to (2.8) for *k=0* and *k=2*: $A_0 = A_2 = -2B_0 = 2B_2 = -2/(RC) = -2\pi f_{rc}$, where $f_{rc}=(\pi RC)^{-1}$ is defined as the 3 dB bandwidth of a single low-pass filter with resistor R/2 and capacitor C (see Fig. 2.5). Applying $v_{in}(t) = Ae^{j2\pi ft}$ as the input in the state equations in (2.8) and also assuming that $\tau_0 = \tau_2$ and $\tau_1 = \tau_3$, we can find $G_k(f)$ in (2.6) for *k=0,1* as:

$$G_0(f) = -\frac{e^{j2\pi(f-nf_s)\tau_0} - e^{-2\pi f_{rc}\tau_0}}{e^{j\pi\frac{f-nf_S}{f_s}} + e^{-2\pi f_{rc}\tau_0}} \cdot \frac{1}{1+j\dfrac{f-nf_s}{f_{rc}}}, \qquad (2.9)$$

$$G_1(f) = -G_0(f)e^{j2\pi f\sigma_2}.$$

Assuming the output voltage is following the voltage on capacitor C_1 during interval k=0, based on (2.8) the Fourier transform of the output can be found as:

$$V_{out,0}(f) = \sum_{n=-\infty}^{\infty} H_{n,0}(f)V_{in}(f-nf_s),$$

$$H_{n,0}(f) = \frac{1}{1+j\dfrac{f}{f_{rc}}} \times \left(\frac{1-e^{-j2\pi nf_s\tau_0}}{j2\pi n} + \frac{1+e^{j2\pi\left((f-nf_s)\tau_1 - nf_s\tau_0\right)}}{2\pi\dfrac{f_{rc}}{f_s}} G_0(f) \right). \qquad (2.10)$$

The output spectrum is the superposition of contributions for all N paths, and taking into account the phase shifts between the contributions the complete output spectrum can be found as:

$$V_{out}(f) = \sum_{n=-\infty}^{\infty} H_n(f)V_{in}(f-nf_s),$$

$$H_n(f) = \sum_{k=0}^{N-1} H_{n,k}(f),$$

$$H_{n,k}(f) = \frac{e^{-j2\pi nf_s\sigma_k}}{1+j\dfrac{f}{f_{rc}}} \times \left(\frac{1-e^{-j2\pi nf_s\tau_k}}{j2\pi n} + \frac{1+e^{j2\pi\left((f-nf_s)(\frac{T_s}{2}-\tau_k)-nf_s\tau_k\right)}}{2\pi\dfrac{f_{rc}}{f_s}} G_{0,k}(f) \right), \qquad (2.11a)$$

$$G_{0,k}(f) = -\frac{e^{j2\pi(f-nf_s)\tau_k} - e^{-2\pi f_{rc}\tau_k}}{e^{j\pi\frac{f-nf_s}{f_s}} + e^{-2\pi f_{rc}\tau_k}} \times \frac{1}{1+j\dfrac{f-nf_s}{f_{rc}}}, \tag{2.11b}$$

According to (2.11) $H_n(f)$ is composed of N components generated by the N paths. We will now derive filter characteristics from (2.11).

2.4 Characteristics of a Differential N-path Filter

2.4.1 Filtering and Harmonic Folding Back Effects

For an ideal N-path filter we assume $\tau_0 = \tau_1 = ... = \tau_{N-1} = \tau = DT_s$, where D is the duty-cycle of the multiphase clock. Analysis of (2.11) shows that $H_n(f)$ is undefined for n=0, but we can take the limit of $H_n(f)$ when "n" approaches continuously to zero to find $H_0(f)$. Moreover, in deriving (2.11) we assumed $D \le (1/N)$ (non-overlapped switching). When $D < (1/N)$, there are periodic time intervals that all the switches are off and the output signal is tracking the input signal (instead of the voltages on the capacitors). The output spectrum contribution generated due to this fact is not considered in (2.11). In order to include this effect in $H_0(f)$, the factor (1-ND) should be added to the part which is derived from (2.11) by taking the limit for "n" to zero. The final result becomes:

$$H_0(f) = \frac{N}{1+j\dfrac{f}{f_{rc}}} \times \left(D + \frac{1+e^{j\pi(1-2D)\frac{f}{f_s}}}{2\pi\dfrac{f_{rc}}{f_s}} \times \left(-\frac{e^{j2\pi D\frac{f}{f_s}} - e^{-2\pi D\frac{f_{rc}}{f_s}}}{e^{j\pi\frac{f}{f_s}} + e^{-2\pi D\frac{f_{rc}}{f_s}}} \cdot \frac{1}{1+j\dfrac{f}{f_{rc}}} \right) \right) + (1-ND). \tag{2.12}$$

Although (2.12) includes the clock duty-cycle effect ($D \le (1/N)$) in the output spectrum, in an ideal N-path filter: $D = (1/N)$. In (2.12) $H_0(f)$ represents the desired filtering characteristic without any frequency translation. $H_0(f)$ for a 4-path filter with the values of D=1/4, R=100 Ω, C=50 pF and f_s=500 MHz is shown in Fig. 2.6.

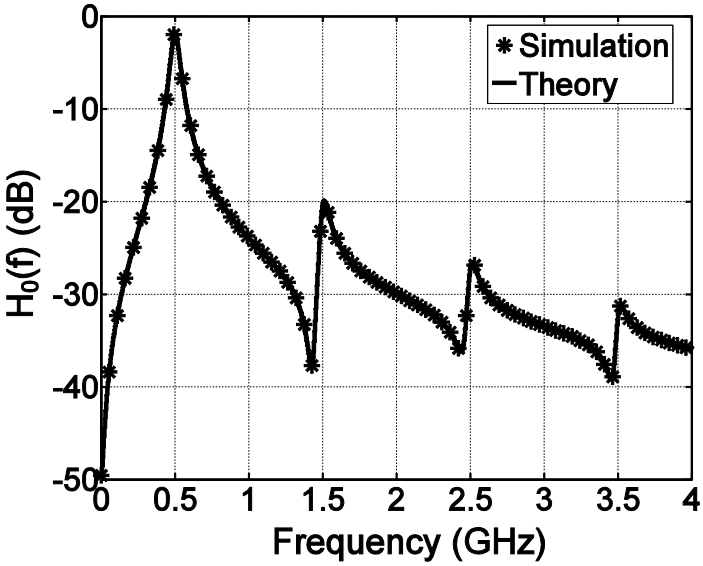

Figure 2.6. Theoretical and simulated curve for $H_0(f)$ at f_s=500 MHz for D=1/4, R=100 Ω and C=50 pF.

In Fig. 2.6 the comparison between the theoretical transfer function from (2.12) and the simulated results applying Spectre-RF PSS-PAC is shown, which fit completely on top of each other. Fig. 2.6 shows bandpass filtering around the switching frequency, for this case with 1.8 dB insertion loss. However, there are also response peaks around odd harmonics of the switching frequency, related to repetitive poles in the denominator of (2.12). Thanks to the differential architecture, peaking around even harmonics does not occur.

From (2.11) we see that $H_n(f) \neq 0$ for $n = kN$ where k=0, ±1, ±2, … and is zero for other values of n. Thus the filter not only shows a comb-filter characteristic, but also "folding back" from input frequencies around $k(N \pm 1)f_s$ to the desired band around f_s. The strongest terms which result in downconversion in a 4-path filter are shown in Fig. 2.7. For instance, k=1 renders non-zero $H_{\pm 4}(f)$, modeling folding from $3f_s$ and $5f_s$ to f_s (both with frequency shift $-4f_s$). For an 8-path architecture the first folding back will happen from $7f_s$. In general, increasing the number of paths will increase the distance between f_s and the first folded component around $(N-1)f_s$.

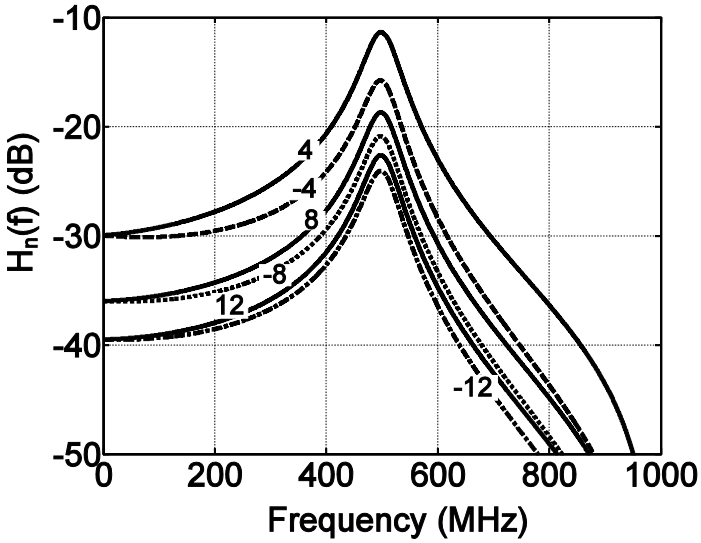

Figure 2.7. $H_n(f)$ around the switching frequency for a 4-path filter. This determines the folding back from odd harmonics of the switching frequency (f_s=500 MHz).

Often, a lowpass pre-filter will be needed in front of the N-path filter to sufficiently suppress harmonic folding. For radio receiver applications, the pre-filter requirements depend on specific blocker scenarios. In fact the folded back power from blockers to the desired band and the amount of degradation in the sensitivity of the receiver must be acceptable. Note that the implementation of a lowpass pre-filter is likely to be feasible, because it doesn't need to be tunable. In the proposed differential N-path filter, second harmonic folding is cancelled which relaxes the pre-filter transition band. Moreover, increasing N can relax the pre-filter transition band requirements.

2.4.2 The Effect of the Switch Resistance

In order to include the effect of the switch resistance in our analysis, we consider the model shown in Fig. 2.8. Since in the architecture illustrated in Fig. 2.3, at any moment just two of the switches are on, the model in Fig. 2.8 includes two switch resistances in front of an ideal N-path filter with zero switch resistances.

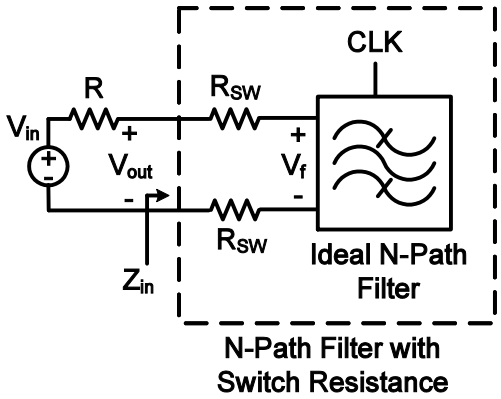

Figure 2.8. N-path filter with switch resistance.

Employing (2.11) with $f_{rc} = (\pi C(R + R_{SW}))^{-1}$, the transfer function from V_{in} to V_f can be easily found. Using superposition of the V_{in} and V_f contributions we find:

$$V_{out}(f) = \frac{2R_{SW}}{R + 2R_{SW}} V_{in}(f) + \frac{R}{R + 2R_{SW}} \sum_{n=-\infty}^{\infty} H_n(f) V_{in}(f - nf_s). \tag{2.13}$$

If R_{SW} is set to zero in (2.13) it returns to the previous form of (2.11). Switch resistance can have strong impact on the maximum achievable rejection in N-path filters. To understand this, consider the frequency transfer function including the switch resistance effect for n=0:

$$H_{0,SW}(f) = \frac{2R_{SW}}{R + 2R_{SW}} + \frac{R}{R + 2R_{SW}} H_0(f). \tag{2.14}$$

According to (2.14), close to the switching frequency the effect of the switch resistance is not significant (H_0 term is close to 1 and dominates). But for frequencies further away from the switching frequency, where $H_0(f)$ is close to zero, the first term often dominates and the output can be approximated as: $V_{out}(f) = (2R_{SW}/(R + 2R_{SW}))V_{in}(f)$. Thus, the maximum filter rejection is limited by the switch resistance, as exemplified by Fig. 2.9 for the same 4-path filter used for Fig. 2.6 but now with R_{SW}=5 Ω added. As a conclusion, in order to increase the maximum rejection of the filter, the switch resistance should be very small with respect to the source resistance R.

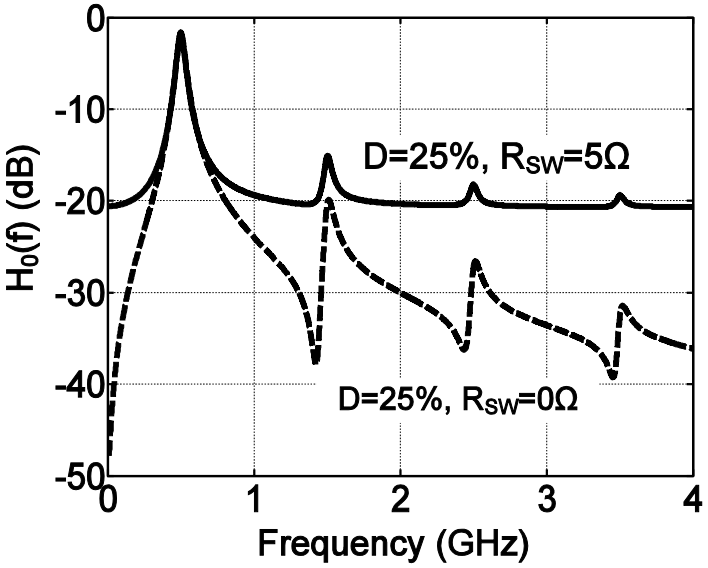

Figure 2.9. Switch resistance effect on the maximum rejection of a 4-path filter (R=100 Ω, C=50 pF, f_s=500 MHz, D=1/4).

2.4.3 Harmonic Selectivity in an N-path Filter

In this section we will discuss the selectivity in the harmonics of the switching frequency both in an analytical and intuitive way. Around filter response peaks, the filter becomes high-ohmic. To quantify the selectivity around the harmonics of the switching frequency, we approximate (2.12) for $f_s >> f_{rc}$, $f \approx nf_s$ for odd n, resulting in:

$$H_0(nf_s) \approx \frac{2N(1-\cos(2\pi nD))}{4D(n\pi)^2} + (1-ND) \qquad 0 < D \le 1/N, \tag{2.15}$$

where n=1, 3, 5,… and $D = \tau / T_s$ is the duty-cycle of each clock phase. As an example, if we substitute N=4 and D=1/4 and n=1, then $H_0(f_s) \approx 8/\pi^2$, i.e. 1.8 dB insertion loss in the pass band, which fits to Fig. 2.6. According to (2.15) increasing N will reduce the insertion loss. As an example, for an 8-path system the insertion loss becomes 0.4 dB. Equation (2.12) was used to produce Fig. 2.10.a, comparing a 4-path and 8-path filter with a fixed total amount of capacitance.

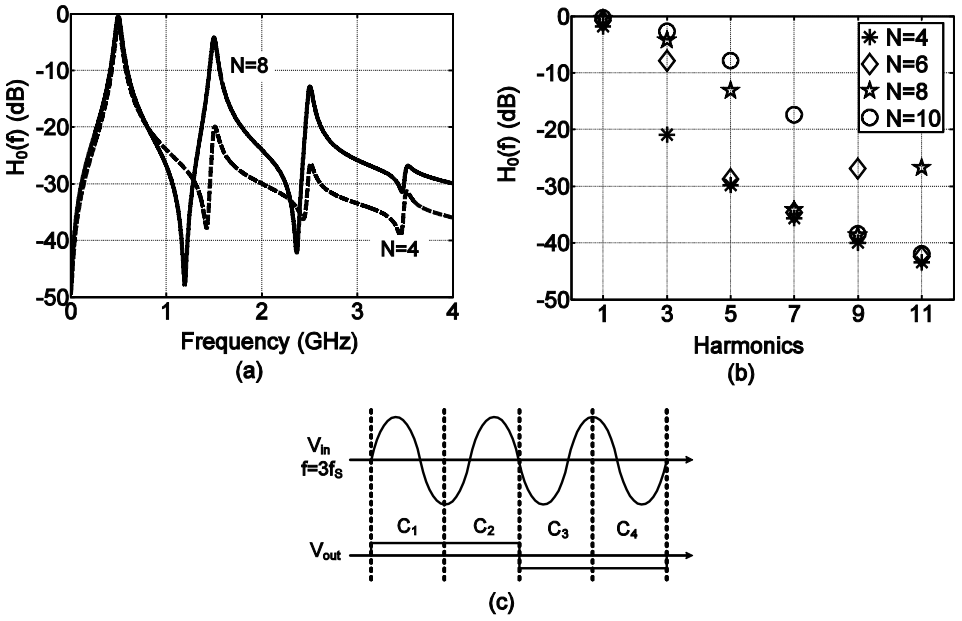

Figure 2.10. (a) Harmonic selectivity comparing the 4-path filter of Fig. 2.6 with an 8-path filter with the same total capacitance (b) Odd harmonic selectivity for different number of paths and D=1/N (eqn. (15)). (c) Waveforms intuitively illustrating 3rd harmonic selectivity and 3rd harmonic folding (down-mixing from $3f_s$ to f_s) for a 4-path filter.

This figure suggests that the filter attenuation around harmonics is reduced by increasing the number of paths. To understand this fact better, notice that the achievable rejection of the filter at the odd harmonics of the switching frequency can be approximated by (2.15). Assuming ideal clocking (substitute D=1/N in (2.15)) the suppression at the harmonics is solely defined by the number of paths. Fig. 2.10.b shows the calculated harmonic rejection applying (2.15). In most cases indeed harmonic suppression decreases by increasing the number of paths, but there are a few exceptions (see Fig. 2.10.b).

To get some intuitive insight how harmonic rejection and harmonic folding occurs, we added Fig. 2.10.c. It shows the time signals for a sine-wave with a frequency of $3f_s$ applied to the 4-path filter of Fig. 2.2.b. Each of the capacitors C_1-C_4 now "sees" the sine-wave for ¾ of a period. The output after integration is a square wave with frequency f_s, which contains both the fundamental and third

harmonic, illustrating that both harmonic selectivity and harmonic folding occurs. Similar signals can be drawn for a larger number of paths. Doing so, we can observe that for more paths, i.e. more number of time slots in Fig. 2.10.c, there is less time to cancel the positive parts of a signal with the negative parts during the integration taking place on each individual capacitor C_1-C_N. Larger N leads to less attenuation of harmonics at the output (Fig. 2.10.b), but less folding back since the stair case approximation in Fig. 2.2.d resembles the actual input signal better.

2.4.4 Input Impedance of an N-path Filter

Now by applying (2.15) we can derive simple expressions for the input impedance of the N-path filter in Fig. 2.8 at the switching frequency, its odd harmonics and for frequencies far away from the peak points in Fig. 2.9. It will be shown that these impedances are all resistive. The effect of the switch resistance can easily be taken into account by substituting (2.15) in (2.14) to find an approximate equation for $H_{0,SW}(nf_s)$. To find the equivalent input impedance of the N-path system $Z_{in}(nf_s)$ we define: $H_{0,SW}(nf_s) = Z_{in}(nf_s)/(Z_{in}(nf_s)+R)$. As a result: $Z_{in}(nf_s) = H_{0,SW}(nf_s)R/(1-H_{0,SW}(nf_s))$. For a 4-path system (N=4, D=1/4) we find:

$$Z_{in}(nf_s) = R_{in}(nf_s) = \frac{8R + (n\pi)^2 R_{SW}}{(n\pi)^2 - 8}. \tag{2.16}$$

Equation (2.16) predicts that at the switching frequency the input impedance of the N-path system is resistive, which is similar to a tank circuit at the resonance frequency. For n=1, (2.16) corresponds to the energy conservation based derivation in [8], but (2.16) can also be used for other values of n. For frequencies far away from the switching frequency and its odd harmonics, using (2.14) we again find purely resistive input impedance:

$$Z_{in}\,|_{\Delta f >> f_s} = R_{in}\,|_{\Delta f >> f_s} = \frac{R + 2R_{SW}}{ND} - R. \tag{2.17}$$

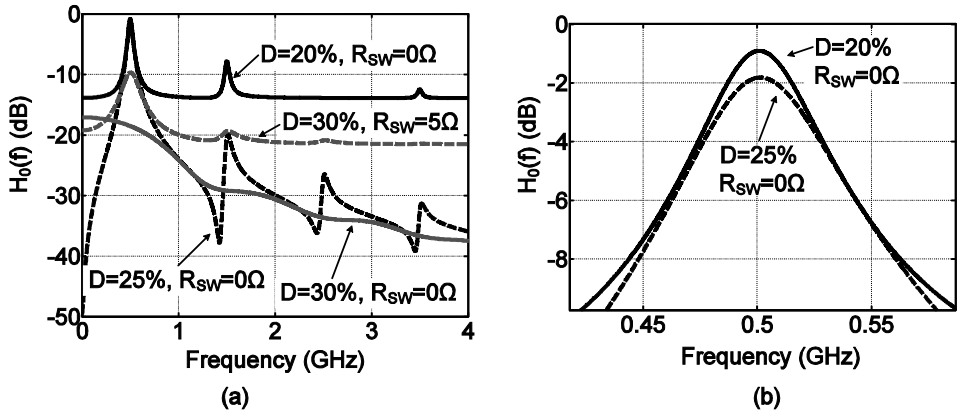

Figure 2.11. (a) Effects of increasing and decreasing of the clock duty-cycle in a 4-path filter. (b) Insertion loss changes due to the duty-cycle reduction.

For an ideal system (D=1/N) (2.17) reduces to $2R_{SW}$. Intuitively this can be understood because the capacitors act like a short circuit for $\Delta f >> f_s$.

We can conclude that at the switching frequency the N-path filter has high impedance (2.16) and for frequencies far away from the switching frequency it renders small impedance (2.17). Later in section 2.4.6 we will apply derivations in (2.15)-(2.17) to derive a simple RLC model for the N-path filter. Moreover, in section 2.5, (2.16) also will be applied to define the required conditions for input power matching.

2.4.5 The Effect of the Duty-Cycle of the Clock

When the duty-cycle of the multiphase clock "D" is smaller than $1/N$, all switches are off periodically for some time and the output signal of the N-path filter simply tracks the (unloaded) input signal. Applying (2.12) for a 4-path architecture, the filter shape for a duty-cycle D=20% is illustrated in Fig. 2.11.a. Comparing to the ideal case (D=25%), notice from (2.17) that reducing the duty-cycle from 1/N results in higher input impedance for the frequencies far away from the switching frequency and its odd harmonics, which translates to less rejection. On the other hand the reduced duty-cycle decreases pass-band insertion-loss, as predicted by (2.12) and also (2.15) (see Fig. 2.11.b). Note that the degradation of the maximum rejection is much more than the reduction in the pass-band loss.

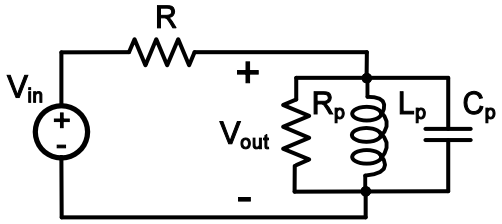

Figure 2.12. Equivalent RLC circuit model for the N-path filter.

As mentioned in section 2.3, our analysis does not include the case $D > (1/N)$ for which two switches can be "on" at the same time, resulting in undesired charge sharing between capacitors. Fig. 2.11.a also shows simulation results for two overlapping clock cases: 1) D=30% and R_{SW}=0 Ω, resulting in complete destruction of the filter shape; 2) D=30%, R_{SW}=5 Ω, where the switch resistance still limits the charge sharing between capacitors and some filtering remains, but with large insertion loss.

2.4.6 RLC Model, Bandwidth and Quality Factor

Around f_s, the filter transfer function $H_0(f)$ as shown in Fig. 2.6 resembles that of a high-Q tank circuit. Now we want to quantify this similarity and find an equivalent RLC model that predicts the quality factor and bandwidth for the N-path filter. Although (2.11) encompasses a repetitive pattern of poles and zeros, we are mostly interested in poles which occur close to the switching frequency. Equating the denominator of $H_0(f)$ in (2.12) to zero ($\exp(s/(2f_s)) + \exp(-2\pi Df_{rc}/f_s) = 0$) to find the poles, we find: $s = -4\pi Df_{rc} + j2\pi(2k+1)f_s$, k=0, ±1, ±2, …, indeed odd harmonics of f_s. In order to make a narrow-band approximation we just consider the poles close to the switching frequency which are: $s = -4\pi Df_{rc} \pm j2\pi f_s$ and set these poles equal to the poles of the transfer function of Fig. 2.12, which is shown in (2.18):

$$H(s) = \frac{s/(RC_p)}{s^2 + (R_p + R)s/(R_pRC_p) + 1/(L_pC_p)}. \qquad (2.18)$$

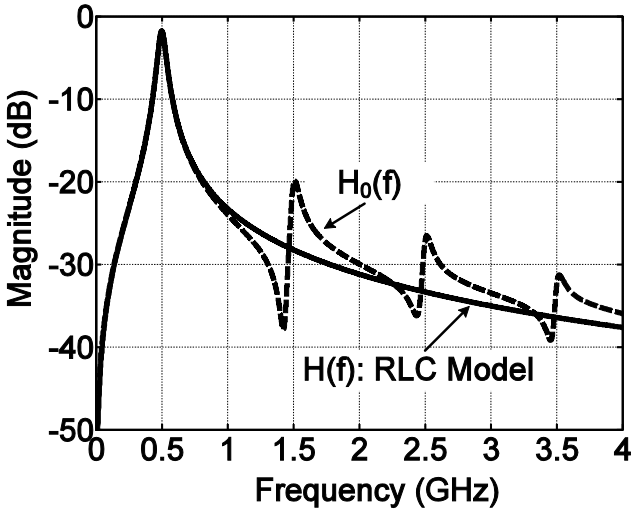

Figure 2.13. Comparison of the transfer of the RLC model with the full N-path filter model (2.11).

As a result C_p and L_p in the RLC model can be found as:

$$C_p = \frac{R_p + R}{8R_pR\pi Df_{rc}}, \tag{2.19a}$$

$$L_p = \frac{1}{4\pi^2 C_p(f_s^2 + 4(Df_{rc})^2)} \approx \frac{1}{C_p(2\pi f_s)^2}. \tag{2.19b}$$

The value of R_p in the RLC model is already derived in (2.16) for a 4-path system with n=1 for the switching frequency. Note that R_p and C_p are independent of f_s, in contrast to L_p. However, the term $4(Df_{rc})^2$ in the denominator of (2.19b) can be non-negligible compared with f_s^2. Thus the maximum in the transfer function can be slightly shifted to higher frequencies which also fits with the N-path filter response. For $f_s >> f_{rc}$ this shift is negligible. To verify the validity of the RLC model, consider a 4-path filter with R=100 Ω and C=50 pF. Employing (2.16) and (2.19) we find C_p=30.8 pF, L_p=3.27 nH, R_p=430 Ω. The comparison between the RLC model and exact transfer function in Fig. 2.13 shows a nearly perfect match around the switching frequency. Applying the RLC model we can find the band-width as: $BW = 1/(2\pi(R \| R_p)C_p) = 4Df_{rc}$. Intuitively this can be understood

considering that in Fig. 2.5 the resistor value charging the capacitor is R/2 and the capacitor sees this resistor value for a fraction 2D of the period, i.e. the "effective resistor" is R/(4D). Therefore the 3 dB bandwidth becomes 4D times the low-pass filter bandwidth defined by f_{rc}. Finally for a 4-path system $BW = f_{rc}$ and $Q = f_s / BW = f_s / f_{rc}$. Thus we see that the bandwidth not only depends on the RC value for each path, but also on the duty-cycle of the clock. Comparing a 4-path (D=1/4) and an 8-path filter (D=1/8) using identical capacitors in each path, the 8-path filter has half the bandwidth of the 4-path filter. If we keep the total amount of capacitance equal, then the bandwidth will not differ by increasing the number of paths (see Fig. 2.10.a). In this chapter we exploit a 1:2 transformer to increase the source resistance, as seen by the filter, and hence reduce the bandwidth and increase the Q of the filter. A further increase in capacitor area can provide even lower bandwidth and higher Q. Notice that as we discussed intuitively in section 2.2, the RC in each path of an N-path filter is performing integration on the input signal, when the corresponding switch is on. In contrast to a sampling system, there is no need for the voltage to settle during one on-time of the switch. Thus the choice of the capacitor size is independent of the switching frequency and can be solely determined based on the desired bandwidth.

2.4.7 Imbalance Multiphase Clocking and Mismatch in the Paths

Next consider what happens if there is mismatch between paths or if clocking signals deviate from the ideal situation. With mismatch, we can expect that even order terms are no longer perfectly cancelled and extra frequency components show up. As an example $H_{\pm 2}(f)$, which was 0 for an ideal N-path system, can be non-zero around the desired band. According to (2.11) this renders an image response (e.g. conversion from $f_{in} = f_s + \Delta f$ to $f_{out} = f_s - \Delta f$) and also folding back from signals around $f_{in} = 2f_s$ to $f_{out} = f_s$. As we use large valued integrated capacitors (10s of pF) good matching is possible and therefore we focus on quantifying clock phase errors. We model clock pulse width variations in the multiphase clocks and apply (2.11), considering unequal pulse widths. Fig. 2.14 shows the calculated image suppression and folding back from $2f_s$. According to Fig. 2.14 one degree of phase error will result in 42 dB of image rejection and 45 dB suppression of second harmonic folding.

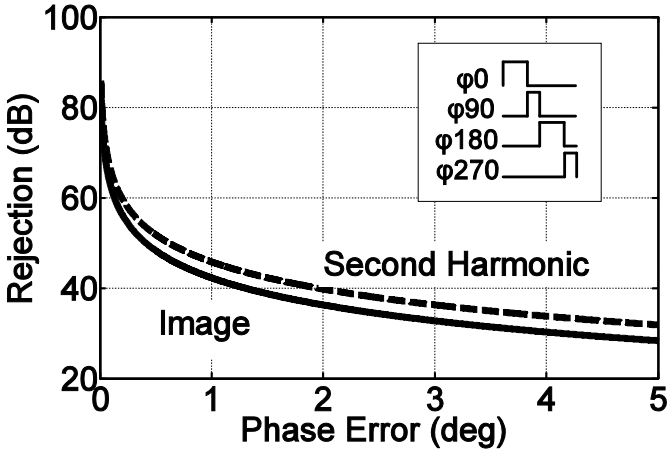

Figure 2.14. Image and second harmonic rejection with phase error in the driving clock phases.

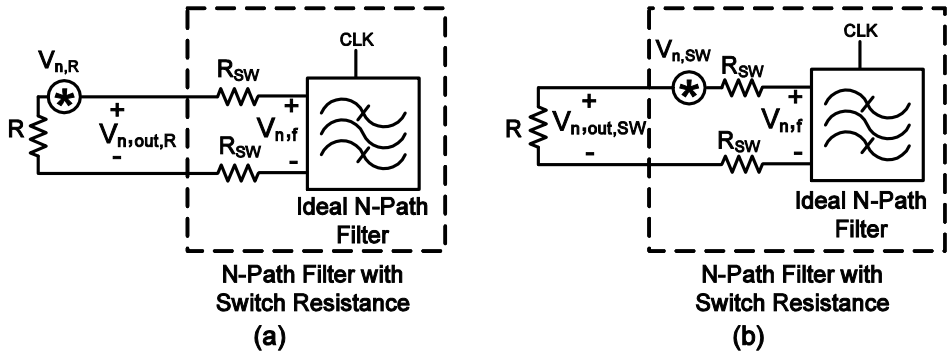

Figure 2.15. The model for noise calculation (a) Source noise (b) Switch resistance noise.

2.4.8 Noise Analysis

Most output noise power is due to the thermal noise of the source and switch resistances, where noise folding from around harmonics of f_s should be incorporated. As the switches do not carry DC current, the flicker noise of the switches can be neglected. At any moment two switches are in the on-state (see Fig. 2.3) and since noise contributions of the switches are not correlated, we can use the model in Fig. 2.15, similar to Fig. 2.8.

As the input impedance around f_s according to (2.16) is significantly bigger than R, the noise voltage source $V_{n,R}$ has a much higher transfer to $V_{n,out}$ than $V_{n,SW}$ has, which is beneficial for noise figure.

Relation (2.13) between the input and output spectrum of an LPTV system can also be applied to random signals. For Fig. 2.15.a we can find $N_{out,R}(f)$, the thermal noise due to R:

$$N_{out,R}(f) = \left|\frac{2R_{SW} + RH_0(f)}{R + 2R_{SW}}\right|^2 N_R(f) + \sum_{n=-\infty, n\neq 0}^{\infty} \left|\frac{R}{R + 2R_{SW}} H_n(f)\right|^2 N_R(f - nf_s). \tag{2.20}$$

The first terms accounts for the noise power which appears at the output without any frequency translation and the second part accounts for noise folding, where $N_R(f - nf_s)$ is the frequency shifted version of the noise power generated by R. Note that $H_n(f)$ in (2.20) can be calculated by applying $f_{rc} = (\pi C(R + R_{SW}))^{-1}$ in (2.11). To calculate the output noise power due to switch resistance we consider Fig. 2.15.b. Similar to the previous case the frequency transfer from $V_{n,SW}$ to $V_{n,f}$ can be calculated from (2.11) with $f_{rc} = (\pi C(R + R_{SW}))^{-1}$. Then by applying the procedure described in section 2.4.2 the transfer function from $V_{n,SW}$ to $V_{n,out}$ can be derived.

Finally for the circuit in Fig. 2.15.b we find:

$$N_{out,SW}(f) = \left(\frac{R}{R + 2R_{SW}}\right)^2 \left(|H_0(f) - 1|^2 N_{SW}(f) + \sum_{n=-\infty, n\neq 0}^{\infty} |H_n(f)|^2 N_{SW}(f - nf_s)\right). \tag{2.21}$$

Again the first part inside the second parenthesis in (2.21) corresponds to the noise power without frequency translation. Since $H_0(f)$ is close to one around the switching frequency for an N-path filter (e.g. 0.81 for a 4-path architecture), the contribution of the first part is very small. The second part in (2.21) is the noise folding term and turns out to be almost negligible. For example, in a 4-path architecture with R_{SW}=5 Ω and R=100 Ω, the noise at the output due to switch resistance is approximately 2% of the total noise at the output. Finally, the noise factor can be calculated as: $F = N_{out}/(A_v^2 N_{in})$.

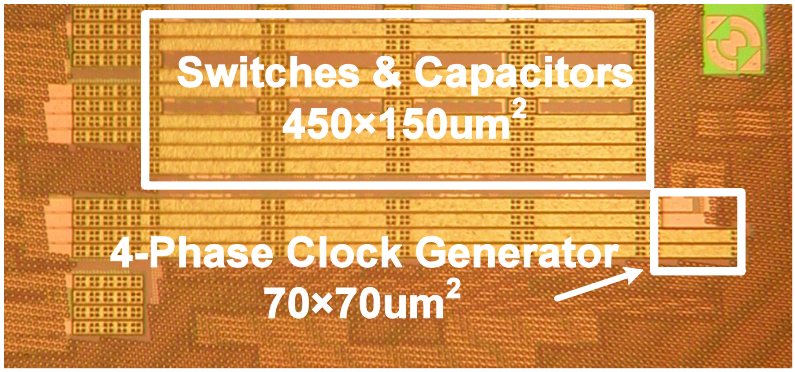

Figure 2.16. Micrograph of the 65 nm CMOS chip.

For a 4-path differential filter with R_{SW}=5, R=100 Ω the calculated noise figure from (2.20), (2.21) is 0.92 dB, which is mainly caused by the noise folding of noise coming from the source resistance R.

2.5 Implementation of a 4-Path Differential Bandpass Filter

A 4-path differential single port filter is realized in 65 nm standard CMOS technology (see Fig. 2.16). The block diagram of the filter is illustrated in Fig. 2.17. Capacitors of 66 pF are realized with NMOS transistors, at 720 mV gate bias (see Fig. 2.18.b), to achieve large capacitance density with good linearity. NMOS switches of W/L=100/0.06 are driven by a 25% duty-cycle 4-phase clocks. The clock phases are capacitively coupled to the gates of the switches which are biased at 950 mV DC voltage to provide full 1.2 V swing on the gate-source nodes of the switches. This swing insures the maximum achievable linearity for switches with fixed sizes. Increasing switch size will improve linearity and decrease the switch resistance. However, larger switch size also means larger parasitic capacitors, affecting the frequency range and clock leakage and also requiring more clock power to drive the switches.

An off-chip wide-band (50-1000 MHz, Mini-Circuits JTX-4-10T) RF transformer serves as a balun for single to differential conversion. Moreover, it increases the impedance level seen by the switched-capacitor circuit, increasing filter-Q without a significant degradation in its noise. The architecture in Fig. 2.17 also has an extra resistor R_M to provide input power matching to 50 Ω. To find the required conditions for power matching we will use (2.16).

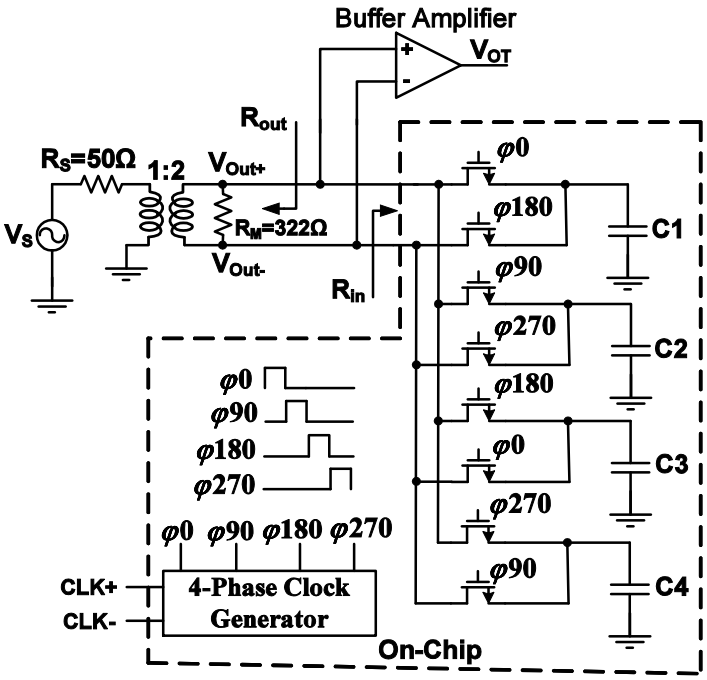

Figure 2.17. Filter architecture including a balun and buffer amplifier for measurements.

Neglecting switch resistance, $R_{in}(f_s)$ "looking into the IC" can be written as: $R_{in} = 8R_{out}/(\pi^2 - 8)$, where R_{out} is the driving impedance seen by the IC (see Fig. 2.17). Then the required value for R_M to provide matching can be found as: $R_M = 4\pi^2 R_s/(16 - \pi^2)$. For Rs=50 Ω the value for R_M becomes 322 Ω. In practice, the insertion loss of the transformer is non-negligible and in our case it was actually sufficient to implement R_M. In the general case an equivalent total resistance R_M according to the derived value is needed for good S_{11}.

The simplified block diagram of the quadrature clock generator with low phase error [13] is shown in Fig. 2.18. A master clock (CLK) at 4 times the switching frequency is applied from off-chip. A flip-flop based divider divides the input clock by four, while an AND-gate between node A and B generates a 25% clock. Finally a shift register implemented with transmission gate flip-flops produces 4-phase clocks to drive the switches. These clocks are then capacitively coupled to the gate of the switches after buffering (see Fig. 2.18.b).

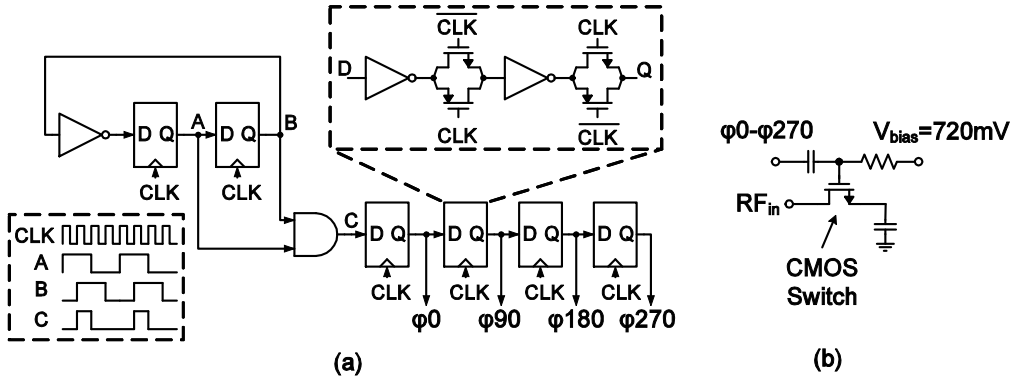

Figure 2.18. Multiphase clock generator.

2.6 Measurement Results and Comparison

An external differential high input impedance buffer amplifier is added in the circuit of Fig. 2.17 to be able to measure with 50 Ω equipment without loading the output of the filter. We utilized Agilent ATF-54143 HEMT transistors to make an amplifier with high linearity and low noise in order to have minimum influence on the measurement results. Measurement results show that the tunable filter in Fig. 2.17 works from 100 MHz up to at least 1 GHz. Fig. 2.19 shows measurement results and compares them to a simulation employing an ideal transformer and R_M=322 Ω for $f_s = 400\,MHz$, while also including a bond-wire inductance estimate. The buffer amplifier gain is de-embedded in all experiments, but the transformer effects are included. Considering the fact that R_{out} in Fig. 2.17 is 123 Ω, R_{SW}≈5 Ω and NMOS capacitors have the value of approximately 66 pF (simulated value), then according to section 2.4.6 the bandwidth is calculated as 36 MHz. The measured value for the bandwidth is 35 MHz which renders a Q ranging from 3 to 29 for f_s ranging between 0.1 and 1 GHz.

As derived in section 2.4.6 the bandwidth of an N-path filter for a given N is a function of the RC-time of the filter. Any variation of R and C will hence result in filter bandwidth deviations from the designed value.

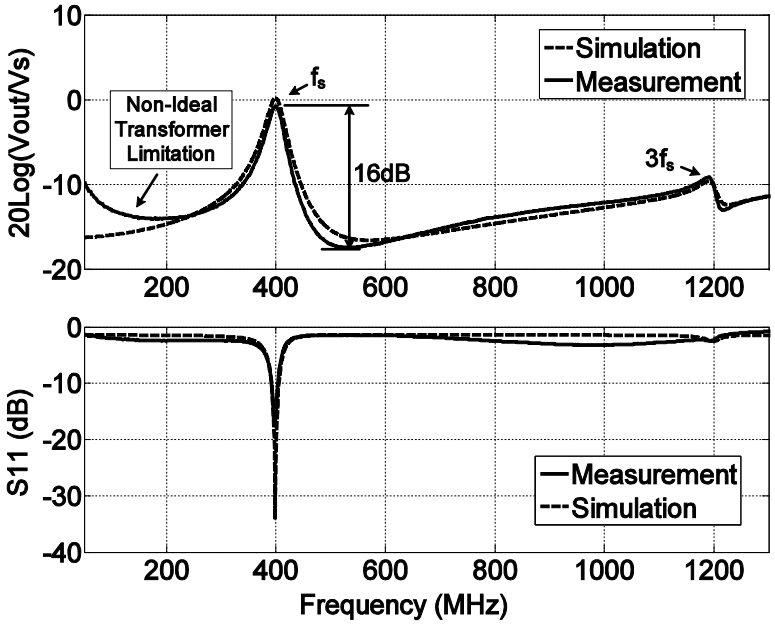

Figure 2.19. Frequency transfer and S_{11} at $f_S = 400\,MHz$.

While changes of C are due to PVT variations, the effective resistance seen by the filter for radio receiver application depends on the effective antenna impedance, which may show significant deviations. As a result a capacitor tuning scheme might be needed to keep the bandwidth fixed over RC variations. The extra switches needed to add or remove capacitors can have larger size than the main clocked switches, since the capacitive switch parasitics can be absorbed in the wanted capacitance. Moreover these switches will be static (don't consume dynamic power). Thus the maximum rejection of the filter will hardly be affected, nor its the noise and linearity.

Close to f_s the input is matched to 50 Ω for a narrow band, simplifying the design of a preceding band-pass or lowpass filter to mitigate the harmonic folding problem. The maximum filter rejection is limited by non-zero switch resistance and impedance R_{out}. Applying (2.17) and considering a 4-path architecture (N=4) and D=0.25 for frequencies far away from the switching frequency, input impedance R_{in} can be approximated as two times the switch resistance R_{SW}.

The maximum rejection, α, can then be estimated as:

$$\alpha \approx 20\log(\frac{\pi^2}{8}\frac{2R_{SW}}{R_{out}+2R_{SW}}). \quad (2.22)$$

Thus increasing R_{out} by applying the transformer not only results in less bandwidth and hence an increased Q, but also larger maximum achievable filter rejection. More attenuation can also be achieved using wider switches at the cost of clock driver power. In the implemented architecture, $R_{SW}\approx 5\ \Omega$, $R_{out}=123\ \Omega$, resulting in α=-20.6 dB. Measurement results render -16 dB (Fig. 2.19).

The difference is likely due to the effect of the non-zero rise and fall times of the clock, reducing in an effective duty-cycle below 25%. According to (2.17) this results in larger input impedance and hence a smaller maximum rejection. Fig. 2.19 also illustrates the frequency selectivity around odd harmonics of the switching frequency. A rejection of 10 dB is found around $3f_s$.

Other harmonic responses are lower than the maximum attenuation (16 dB) posed by the switch resistance and parasitics of the board, and are not observable in the measurement results.

Fig. 2.20 compares the calculated and measured values for folding back from all of the harmonics of f_s up to 15th. In this measurement the switching frequency is taken to be 100 MHz and we have removed the transformer and applied a microwave hybrid with wider frequency band in order to remove the bandwidth limitation from the transformer. For odd harmonics the deviation between measurement and calculated results is due to band limitation imposed by the parasitics of the input of the chip. Even order harmonics are rejected ideally, but mismatch and clock errors limit the rejection. Fig. 2.20 shows that spectral aliasing from even harmonics is better than -60 dB.

Measurement results of the in-band image rejection are presented in Fig. 2.21 and prove to be better than 50 dB. The differential architecture also reduces the power leakage from the switching clock to the RF input. In Fig. 2.17, the rising and falling edges of the clock mainly produce a common mode signal, which is suppressed by the common mode rejection of the transformer. At the RF input, a clock leakage power or LO radiation of <-62 dBm was measured over the whole band. This is lower than the -57 dBm spurious domain emission limit for frequencies below 1 GHz, as specified by FCC part 15 [14].

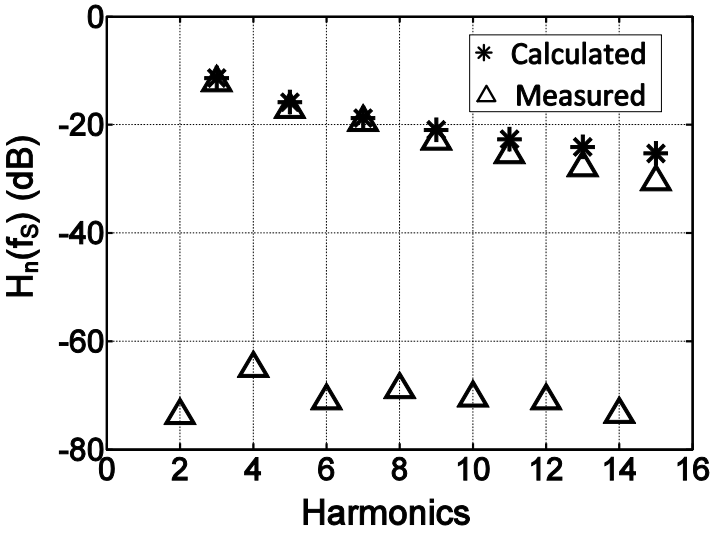

Figure 2.20. Folding back from harmonics at $f_s = 100\,MHz$ (measured and calculated with (2.11); even harmonics ideally are fully cancelled).

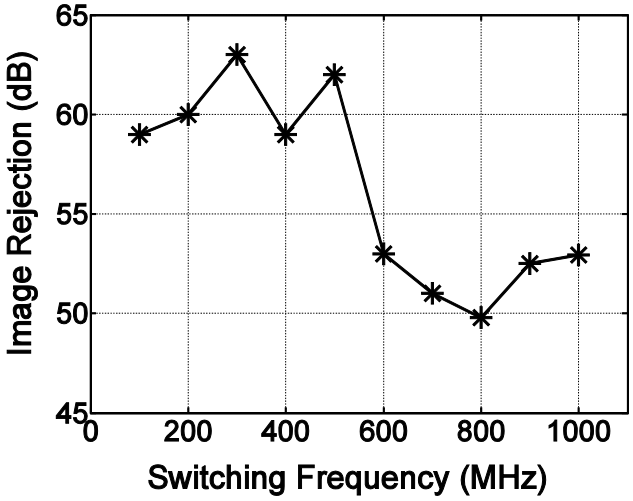

Figure 2.21. Measured in-band image rejection for $f_s = 0.1 - 1GHz$.

Moreover, if a pre-filter is deployed before the N-path filter, the leaked power at harmonics of the switching clock will be suppressed. Note also that in a cognitive radio application, the fundamental LO-leakage constitutes self-interference.

Monte Carlo simulation of process and mismatch variations predict -78 dBm clock leakage in the worst case (100 runs), which suggests that other factors like coupling between wires and substrate may dominate the LO-leakage. Better layout may provide less leakage due to coupling.

The flexible tuning capability of the filter is illustrated in Fig. 2.22 for f_s swept from 100 MHz up to 1 GHz. In-band S_{11} proves to be better than -10 dB and the voltage transfer characteristic exhibits a maximum of 2 dB pass-band attenuation over the entire tuning range. Due to parasitics of the transformer and PCB some peaking occurs at 100 and 200 MHz center frequencies. The main frequency limitations of the current design are related to the clocking circuit and transformer. Wider frequency ranges are possible by improving the clocking circuit and removing the transformer for on-chip applications. The implemented 4-phase clock generator consumes between 2 mW and 16 mW ($f_s = 0.1-1\,GHz$, $f_{CLK} = 0.4-4\,GHz$). The rest of the circuit is free of dissipation from the supply.

Around the switching frequency the N-path filter has high input impedance ($4.3R_S$ in a 4-path filter). Thus not much current flows through the filter and one might intuitively expect good linearity, certainly for large switch-overdrive voltages (≈800 mV). Fig. 2.23 shows IIP3 measurement results where the worst value within the 3 dB bandwidth is reported. It is always better than 14 dBm.

As derived in section 2.4.8, the noise figure of a 4-path filter without transformer and matching resistance is 0.9 dB, which fits to "Spectre-RF" transistor level simulation results in Fig. 2.24-case 1. For the architecture in Fig. 2.17 that we have applied for the measurement, assuming an ideal 1:2 transformer, the value of R in (2.20) and (2.21) becomes equal to R_{out}=123 Ω (see Fig. 2.17). Considering unity voltage gain (V_{out}/V_S=1) for the matched input and calculating the noise power from (2.20) and (2.21), a noise figure of 3 dB is calculated, again equal to simulation (Fig. 2.24-case 2). In Fig. 2.24 measurement results (the buffer amplifier noise figure is de-embedded) are shown as case 3 which shows an increasing trend of NF at high frequencies.

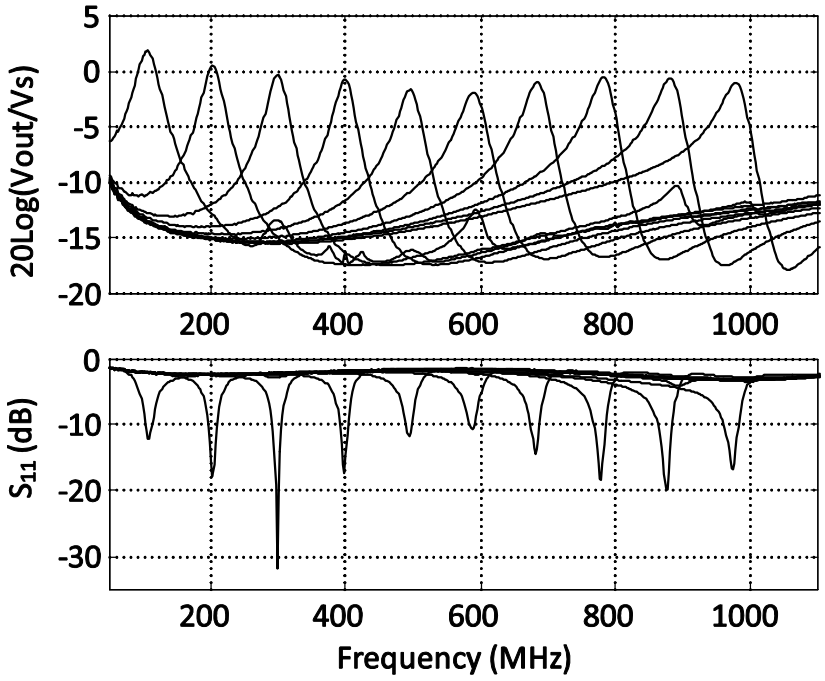

Figure 2.22. Frequency transfer and S_{11} at f_s between 0.1 and 1 GHz.

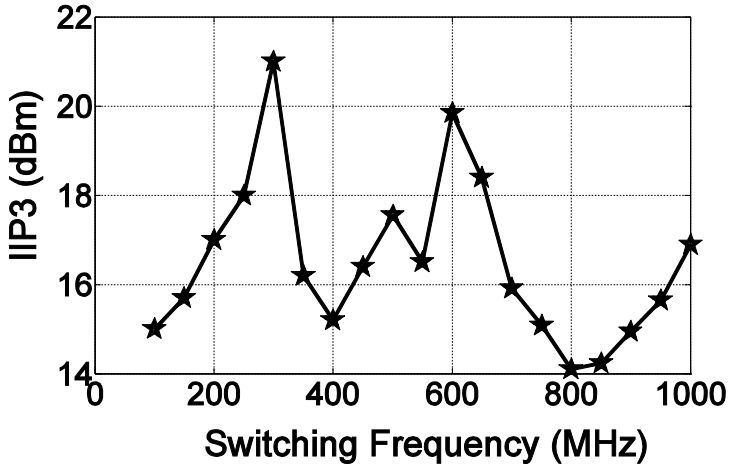

Figure 2.23. Measured minimum IIP3 for $f_s = 0.1 - 1GHz$.

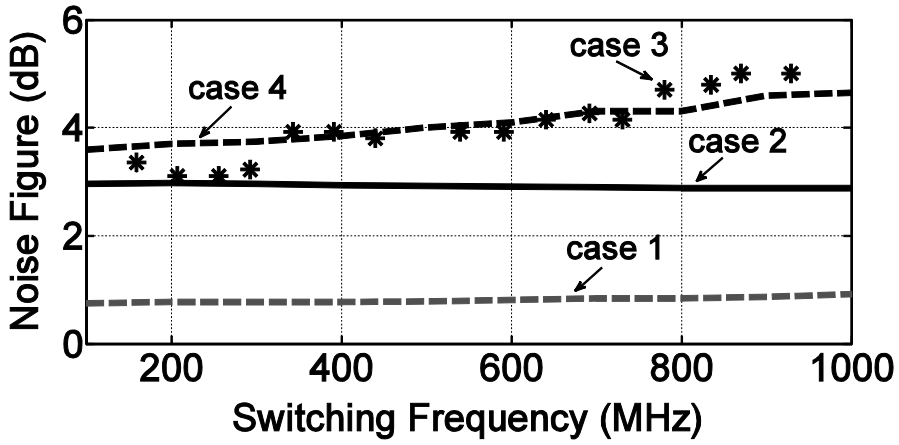

Figure 2.24. Measured and simulated noise figure: case 1- Simulation of the un-matched 4-path filter without the transformer and matching resistor; case 2- Simulation with ideal transformer and matching resistor included; case 3- Measurement of the setup in Fig. 2.17; case 4- The effect of the stray inductance of the transformer is included in the simulation of case 2.

Simulations show that stray inductance in the transformer and PCB lines lead to an increment of noise figure at high frequencies. Modeling the stray inductance in the secondary of the transformer, R_{out} in Fig. 2.17 should be replaced by an impedance which increases with frequency. In this case the noise generated by the switch resistances at the output node can no longer be neglected resulting in a noise power increasing with frequency. In Fig. 2.24-case 4 the simulation of an ideal transformer with matching resistance R_M=322 Ω and 8 nH stray inductance in series with the secondary winding of the transformer is shown. Fitting a coupled inductor model with finite coupling factor to a 50 MHz-1 GHz bandwidth transformer indicates that such inductance values are in the realistic range.

In table I the design is compared with two other on-chip filters, one using Q-enhancement [15] and the other an 8-path filter [5], clearly illustrating benefits in tuning-range, linearity and noise. In [5] the achieved Q is increased significantly by increasing source resistance and also increasing the total capacitance value without providing matching. Inserting a resistor deteriorates the NF significantly. Reactive impedance transformation as employed here ensures a low NF.

Table 2.1. Comparison with other designs.

Performance	This Work	[5]	[15]
Process	65 nm CMOS	0.35 um CMOS	0.18 um CMOS
Active Area	0.07 mm^2	1.9 mm^2	0.81 mm^2
Power Consumption	2 to 16 mW	63 mW	17 mW
Frequency Tuning Range	0.1 to 1 GHz	240 to 530 MHz	2 to 2.06 GHz
-3dB Band Width	35 MHz	1.75 to 4.6 MHz	130 MHz
Voltage Gain	-2 dB	-2 dB	0 dB
Quality Factor (Q)	3 to 29	301 to 114	15.4 to 15.8
P_{1dB}	2 dBm	-5 dBm	-6.6 dBm
IIP3	14 dBm	NA	2.5 dBm
Noise Figure	3-5 dB	9 dB	15 dB

2.7 Conclusions

In this chapter an integrated tunable bandpass filter based on N-path periodically time variant networks is analyzed, implemented and measured. The proposed differential 4-path architecture provides a high-Q inductor-less filter with a decade tuning range (0.1-1 GHz). The availability of high quality switches in CMOS technology offers high linearity ($\geq$ 14 dBm) and compression point (2 dBm). According to theory and measurement, the architecture can have low noise as well (theoretically close to 1 dB for the unmatched case, 3 dB for the matched case). A drawback of N-path filtering is the harmonic folding associated with their time-variant nature. To suppress folding products, a lowpass pre-filter can be used, which however doesn't need to be tunable. In the proposed differential N-path filter, second

harmonic folding is cancelled which relaxes the pre-filter transition band. Further transition band extension is possible using higher N.

As N-path filters outperform most receivers in terms of compression point and IIP3, they are one of the few options compatible with CMOS integration to protect receivers against strong blockers. We believe that their extreme tunability by a digital clock and their high linearity and compression point are attractive assets for software-defined or cognitive radio applications.

2.8 References

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Chapter 3

Tunable N-Path Notch Filters for Blocker Suppression: Modeling and Verification

3.1 Introduction

The demand for multi-mode multi-band wireless handheld devices has been pushing the integration of many wireless transceivers on a single RFIC chip, leading to a reduction in cost, size and power consumption. However, close proximity of wireless transceivers, which are also supposed to work concurrently, poses a very challenging coexistence problem: the transmitted signal of one transmitter becomes a "blocker" for co-existing receivers (see Fig. 3.1.a), which can be stronger than 0 dBm. A somewhat similar problem occurs in a single standard wireless systems with frequency division duplexing (FDD) where the receiver and the transmitter share the same antenna through a duplexer as shown in Fig. 3.1.b (e.g. W-CDMA). Although, the duplexer provides some selectivity still leakage of the transmitted power to the receiver can deteriorate the sensitivity of the receiver.

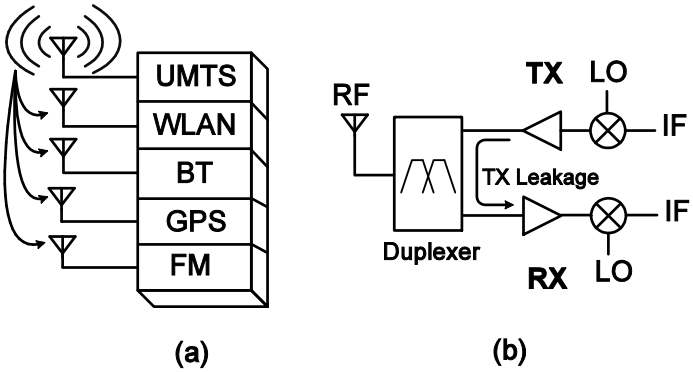

Figure 3.1. Coexistence problem in (a) Multi-standard system (b) A frequency division duplexing (FDD) system.

Similar challenges also occur when aiming at Dynamic Spectrum Access, exploiting software defined radio concepts. In order to provide suppression for blockers, a notch filter can be applied in the receiver. A high-Q filter is needed, e.g. 10 MHz bandwidth around 1 GHz asks for a Q of 100. Given the desire to support multiple radio bands, a software-defined radio solution is preferred, i.e. a filter which is widely tunable in a digitally controlled way.

A well-known way to implement a high-Q notch filter is by applying an LC resonator assisted with a Q-enhancement negative impedance circuit to overcome the limited Q of on-chip inductors (see Fig. 3.2.a) [1]. Apart from consuming a large die area, these circuits suffer from limited linearity due to the application of active components in the negative impedance circuit. Moreover the tunability, usually implemented with varactors, is limited and makes the bandwidth of the notch filter frequency dependent. Finally the center frequency is strongly related to the process variations and parasitics which makes the design even more difficult.

Another approach to realize a bandstop filter is applying the frequency-translated filtering [2-14]. As an example in [3] the low input impedance of a trans-impedance amplifier with feedback is upconverted to create a notch filter at low frequencies (80 MHz) suppressing TX leakage in an FDD system (see Fig. 3.2.b). In [15] we presented a differential and a single-ended (SE) 8-path notch filter. These switched-RC 8-path notch filters demonstrate a very high-Q bandstop characteristic with a center frequency determined by the switching frequency which can have a very low sensitivity to the PVT (Process, Voltage, and Temperature) variations.

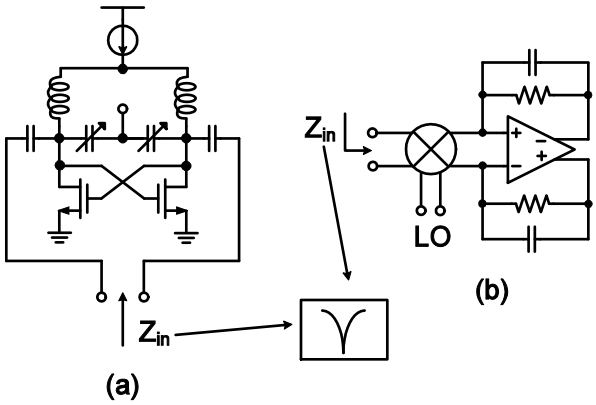

Figure 3.2. (a) LC Q-enhanced notch filter [1] (b) Frequency translated notch filter [3].

To exploit N-path filters, we need a clock and the question arises how to realize this clock. If we aim at rejecting a "self-blocking" transmitter signal, this can be relatively straightforward as the synthesized frequency is readily available. However, if we aim at applying N-path notch filters for Dynamic Spectrum Access applications, we need information about the blocker frequency. This information can come from databases that are currently built [16] or from spectrum sensing, see for instance [17, 18]. The clock generation will require extra hardware in the system. Note that apart from N-path filters, there are hardly other integrated filter techniques that can handle 0dBm blockers while also providing tunable filtering. This is especially true at low GHz frequencies, where inductor takes large chip area and have rather poor quality factor. On the other hand new CMOS technologies offer high density linear capacitors and switches with low "on" resistance, low nonlinearity and low parasitic capacitance. This allows for realizing purely passive notch filters with high linearity and large blocker handling capability.

In this chapter we provide an elaborate analysis of N-path notch filters with closed form equations. The analysis results describe the main characteristics of the notch filters such as bandwidth and maximum rejection at notch frequency. They also provide comprehensive quantitative results for non-ideal properties of the N-path notch filters such as harmonic mixing, the effect of the switch resistance, reduced duty-cycle, pass-band insertion loss, noise figure, mismatch and phase imbalance. Similar to the N-path bandpass filters discussed in previous chapter a simple RLC model is presented for the frequencies close to the switching frequency which describes the main properties of the N-path filters in a quite simple but rather accurate manner.

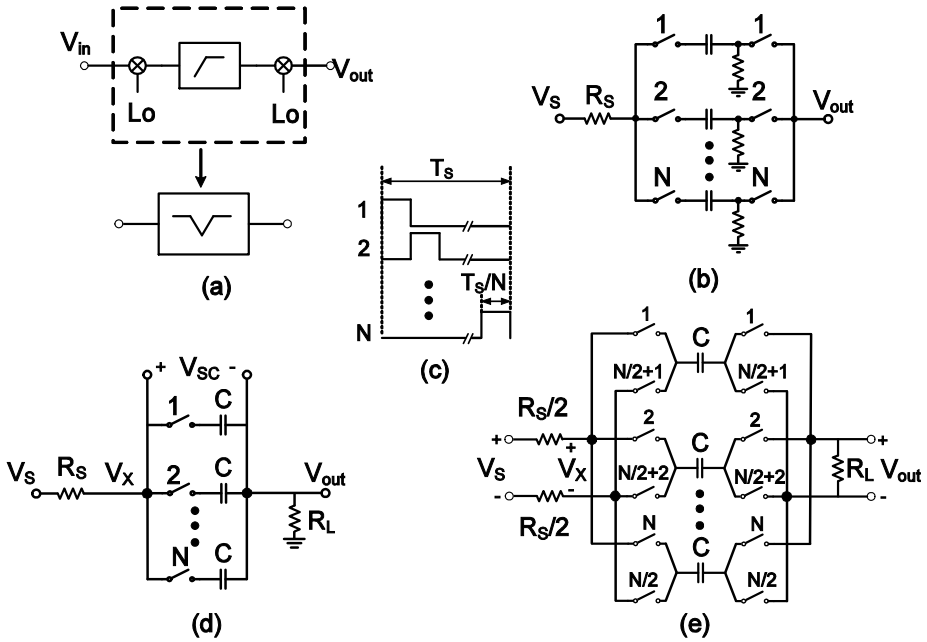

Figure 3.3. (a) Upconverted high-pass filter represents a notch filter at LO. (b) Single-ended (SE) N-path notch filter. (c) Multiphase clock which drives the switches in the N-path filter. (d) Simplified SE N-path filter. (e) Differential N-path filter.

Measurement results will also be provided for the 8-path notch filters, most notably transfer function and notch depth measurements under strong blocking conditions. In section 3.2 a short intuitive introduction of N-path notch filters is presented, while section 3.3 covers the mathematical analysis. In Section 3.4 important non-idealities of the N-path notch filters are discussed based on the analysis results of section 3.3. Sections 3.5 and 3.6 cover the implementation and measurement results of notch filters, while section 3.7 presents conclusions.

3.2 N-Path Notch Filter Concept

Fig. 3.3.a illustrates how upconverting a highpass filter characteristic in the baseband to the LO frequency results in a bandstop or notch behavior. The highpass filter can be as simple as a C-R network (Fig. 3.3.b) and the mixers in Fig. 3.3.a can be realized by switches driven by multiphase clocks (Fig. 3.3.c).
The resistances of the highpass filters in Fig. 3.3.b are not memory elements and only one path is active at any time, so one shared resistor can be used (Fig. 3.3.d).

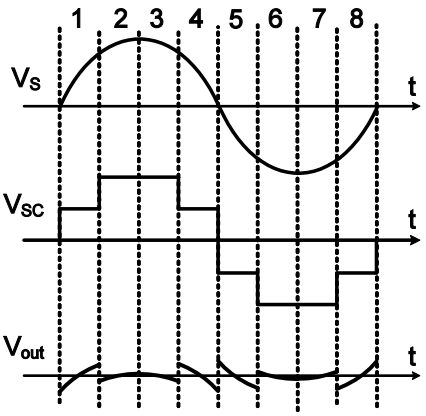

Figure 3.4. A typical timing diagram of the input-output voltages in an 8-path notch filter with a sine wave input signal with a frequency equal to the clock frequency of the switches.

In each path one of the two switches can be removed if we assume the clock phases driving the two involved switches are the same. Thus the simple single-ended (SE) notch filter shown in Fig. 3.3.d results. Considering the single-ended N-path notch filter in Fig. 3.3.d for N=8, a typical set of node voltages for a sinusoidal signal with the frequency of the switching frequency as an input is illustrated in Fig. 3.4. Here we assume that the RC time constant is very much larger than the closing time of the switches, then the voltages on the capacitors contains approximately a constant value which is the integration of the part of the input signal seen periodically by each capacitor. The passive mixers which are realized by the switches, upconvert the DC voltages on the capacitors and create a stair case approximation of the input signal on the switched-capacitor part in Fig. 3.3.d as V_{SC}. The output voltage $V_{out} = (R_L /(R_L + R_S))(V_S - V_{SC})$ in Fig. 3.4 illustrates a strong suppression of the input signal.

As a result the switched-capacitor part in combination with the source and load resistors act as a high impedance element for the switching frequency while it presents a low impedance for the frequencies far away from the switching frequency. However, note that this circuit not only will present a notch characteristic at the switching frequency but also at the harmonics of the switching frequency. At first sight this may seem similar to some comb filters or microwave filters, but here it results from mixing effects and the clock periodicity defines the frequency spacing. Note also that apart from repeated filter responses, the mixing nature of the circuit

also introduces unwanted mixing products. These will be analyzed later in this chapter. A fully differential N-path notch filter architecture is shown in Fig. 3.3.e. A second set of switches is required to generate the differential signal at the output. As a result of the fully differential structure, the notch behavior at the even harmonics of the switching frequency is cancelled, so the pass-band is widened compared to the single-ended version. Despite the unwanted responses, the N-path filters can achieve very high Q, whereas they are digitally tunable in the center frequency by simply changing the mixer clock frequency. However, insight in several second order effects is needed to successfully apply N-path circuits, and we hope to provide such insight and quantitative estimates for filter properties in this chapter.

3.3 Mathematical Analysis

3.3.1 State-Space Analysis

In previous chapter we provided the detailed analysis results for the differential N-path bandpass filter. Here we will follow the same analysis approach to derive the transfer functions for the SE and the differential notch filters. The circuits shown in Fig. 3.3 are Linear Periodically Time Variant (LPTV) systems. If we define the voltage on the switched-capacitor part as: $V_{SC}(f) = V_X - V_{out}$, it can be shown that the relation between $V_{SC}(f)$ and the input in such an LPTV circuit will comply with the following equation [19, 20]:

$$V_{SC}(f) = \sum_{-\infty}^{\infty} H_n(f) V_S(f - nf_s), \tag{3.1}$$

where f_s is the switching frequency, "n" indicates a harmonic of f_s and $H_n(f)$ is the "harmonic transfer function" associated with the frequency shift of nf_s. Equation (3.1) models the frequency spectrum for $V_{SC}(f)$ as a summation of shifted versions of the input spectrum multiplied by a weighting factor $H_n(f)$. Once we find $V_{SC}(f)$ then the output spectrum relates to the input as following:

$$V_{out}(f) = \frac{R_L}{R_L + R_S}\left(V_S(f) - V_{SC}(f)\right) = \frac{R_L}{R_L + R_S} \times \left(\left(1 - H_0(f)\right) V_S(f) - \sum_{n=-\infty, n\neq 0}^{\infty} H_n(f) V_S(f - nf_s) \right). \tag{3.2}$$

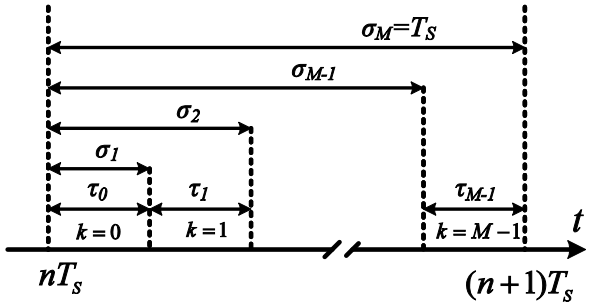

Figure 3.5. Time intervals for the state-space analysis.

According to (3.2) the output voltage on R_L consists of two parts: 1) the desired part "$V_{de}(f)$" which provides filtering without frequency shifting, and 2) "$V_{un}(f)$" which entails possible folding back components that might fall in the desired band. Then $V_{out}(f) = V_{de}(f) + V_{un}(f)$, with:

$$V_{de}(f) = \frac{R_L}{R_L + R_S}\left(1 - H_0(f)\right)V_S(f), \tag{3.3}$$

$$V_{un}(f) = \frac{-R_L}{R_L + R_S}\left(\sum_{n=-\infty, n\neq 0}^{\infty} H_n(f)V_S(f - nf_s)\right). \tag{3.4}$$

As shown in previous chapter, a state-space analysis can be carried out on a single path of an N-path system and by considering the fact that the output spectrum for an N-path system is the superposition of the responses of "N" similar paths after appropriate phase shifting, the frequency response for $V_{SC}(f)$ can be determined. This is possible because we assume that the state variables do not have any interaction with each other and are determined independently from each other. The timing diagram for the analysis is shown in Fig. 3.5. The time interval $nT_s < t < nT_s + T_s$. $T_s = 1/f_s$ is divided into M portions (M is the number of the states) and each portion identified by k can be represented as $nT_s + \sigma_k < t < nT_s + \sigma_{k+1}$, k=0,…, M-1 and $\sigma_0 = 0$ (see Fig. 3.5). During each interval there is no change in the state of the switches and the network behaves as an LTI system. Suppose $\tau_0, \tau_1, \ldots, \tau_{N-1}$ are the time intervals in which each switch is closed. Here we have assumed that there is no overlap in the multiphase clocks and also that $\tau_0 + \tau_1 + \ldots + \tau_{N-1} = T_s$ (later this assumption will be modified to cover the case of a duty-cycle lower than 1/N). By applying

the state-space analysis for the SE N-path notch filter we find the harmonic transfer function of $H_{n,SE}(f)$ in (3.1) as :

$$H_{n,SE}(f)=\sum_{k=0}^{N-1}H_{n,k,SE}(f),$$

$$H_{n,k,SE}(f)=\frac{e^{-j2\pi nf_s\sigma_k}}{1+j\dfrac{f}{f_{rc,SE}}}\times\left(\frac{1-e^{-j2\pi nf_s\tau_k}}{j2\pi n}+\frac{1-e^{j2\pi\left((f-nf_s)(T_s-\tau_k)-nf_s\tau_k\right)}}{2\pi\dfrac{f_{rc,SE}}{f_s}}G_{SE}(f)\right),$$

$$G_{SE}(f)=\frac{e^{j2\pi(f-nf_s)\tau_k}-e^{-2\pi f_{rc}\tau_k}}{e^{j2\pi\frac{f-nf_s}{f_s}}-e^{-2\pi f_{rc}\tau_k}}\times\frac{1}{1+j\dfrac{f-nf_s}{f_{rc,SE}}},$$

(3.5)

where $f_{rc,SE}=1/(2\pi(R_S+R_L)C)$. For the differential circuit in Fig. 3.3.e the state-space analysis results in the following for $H_{n,D}(f)$ in (3.1):

$$H_{n,D}(f)=\sum_{k=0}^{N-1}H_{n,k,D}(f),$$

$$H_{n,k,D}(f)=\frac{e^{-j2\pi nf_s\sigma_k}}{1+j\dfrac{f}{f_{rc,D}}}\times\left(\frac{1-e^{-j2\pi nf_s\tau_k}}{j2\pi n}+\frac{1+e^{j2\pi\left((f-nf_s)(\frac{T_s}{2}-\tau_k)-nf_s\tau_k\right)}}{2\pi\dfrac{f_{rc,D}}{f_s}}G_D(f)\right),$$

$$G_D(f)=-\frac{e^{j2\pi(f-nf_s)\tau_k}-e^{-2\pi f_{rc,D}\tau_k}}{e^{j\pi\frac{f-nf_s}{f_s}}+e^{-2\pi f_{rc,D}\tau_k}}\times\frac{1}{1+j\dfrac{f-nf_s}{f_{rc,D}}},$$

(3.6)

in which $f_{rc,D}=1/(\pi(R_S+R_L)C)$. Please note that $f_{rc,D}$ for the differential circuit is larger than its counterpart ($f_{rc,SE}$) for the SE circuit and this is due to the fact that the effective resistance seen by the capacitors is halved for the differential

circuit. For an ideal N-path filter we assume $\tau_0 = \tau_1 = ... = \tau_{N-1} = \tau = DT_s$ in Fig. 3.5, where $D = (1/N)$ is the duty-cycle of the multiphase clocks. So far we have developed $H_n(f)$ in the general form for both differential and the single-ended circuits in (3.1). We will now derive equations for $H_0(f)$ to find the desired part of the transfer function in (3.3). Analysis of (3.5) and (3.6) shows that $H_{n,SE}(f)$ and $H_{n,D}(f)$ are undefined for *n*=0, but we can take the limit of (3.5) and (3.6) when "*n*" approaches continuously to zero to find $H_{0,SE}(f)$ and $H_{0,D}(f)$. Moreover, in deriving (3.5) and (3.6) we assumed $D = (1/N)$ (non-overlapped switching). When $D < (1/N)$, there are periodic time intervals that all of the switches are off and $V_{SC}(f)$ is tracking the input signal. The output spectrum contribution generated due to this fact is not considered in (3.3). In order to include this effect in $H_{0,SE}(f)$, the factor (1-ND) should be added to the part which is derived from (3.5) by taking the limit for "n" to zero. Finally for the single-ended filter we find:

$$H_{0,SE}(f) = \frac{N}{1 + j\dfrac{f}{f_{rc,SE}}} \times \left(D + \frac{1 - e^{j2\pi(1-D)\frac{f}{f_s}}}{2\pi\dfrac{f_{rc,SE}}{f_s}} \times \left(\frac{e^{j2\pi D\frac{f}{f_s}} - e^{-2\pi D\frac{f_{rc,SE}}{f_s}}}{e^{j2\pi\frac{f}{f_s}} - e^{-2\pi D\frac{f_{rc,SE}}{f_s}}} \cdot \frac{1}{1 + j\dfrac{f}{f_{rc,SE}}} \right) \right) + (1 - ND). \tag{3.7}$$

Similar to the single ended version $H_{0,D}(f)$ for an ideal differential N-path filter can be found as:

$$H_0(f) = \frac{N}{1 + j\dfrac{f}{f_{rc,D}}} \times \left(D + \frac{1 + e^{j\pi(1-2D)\frac{f}{f_s}}}{2\pi\dfrac{f_{rc,D}}{f_s}} \times \left(-\frac{e^{j2\pi D\frac{f}{f_s}} - e^{-2\pi D\frac{f_{rc,D}}{f_s}}}{e^{j\pi\frac{f}{f_s}} + e^{-2\pi D\frac{f_{rc,D}}{f_s}}} \cdot \frac{1}{1 + j\dfrac{f}{f_{rc,D}}} \right) \right) + (1 - ND). \tag{3.8}$$

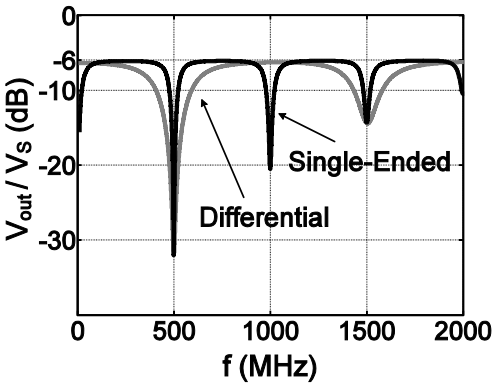

Figure 3.6. The Single-ended and differential 8-path notch filter transfer function for C=7 pF and R_S=R_L=50 Ω

Fig. 3.6 shows the transfer curves of a single-ended and differential 8-paths filters with C=7 pF and R_S=R_L=50 Ω applying equations (3.3), (3.7) and (3.8). These results fall exactly on top of the simulation results carried out with pss-pac in Spectre-RF with ideal capacitors and switches.

3.3.2 RLC Model for Single-Ended Notch Filter

As we showed for the N-path differential bandpass filter in previous chapter, the switched capacitor part can be modeled as a parallel tank circuit for the frequencies close to the switching frequency. Here we provide the RLC model in general and simplified form for the single-ended and differential notch filter. Parallel tank model circuits are shown in Fig. 3.7 for the N-path notch filters. To find the parallel resistance R_P we approximate $H_{0,SE}(f)$ and $H_{0,D}(f)$ in (3.7) and (3.8) for $f_s >> f_{rc}$, $f \approx nf_s$ for all values of n, resulting in:

$$H_{0,SE}(nf_s) = H_{0,D}(nf_s) \approx \frac{2N(1-\cos(2\pi nD))}{4D(n\pi)^2} + (1-ND) \qquad 0 < D \le 1/N. \qquad (3.9)$$

Equation (3.9) is the same for both the differential and the single-ended circuits with only one difference that for the differential circuit it is valid only for odd values of "n". In (3.9) if n=1 then the impedance of the switched-capacitor circuit for the switching frequency can be found as $Z_{in,SE}(nf_s) = H_{0,SE}(f_s)(R_S + R_L)/(1 - H_{0,SE}(f_s))$.

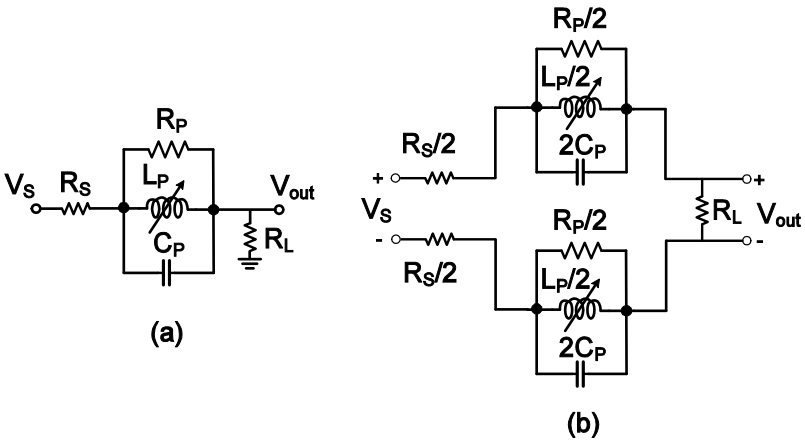

Figure 3.7. RLC model of the ideal single-ended and differential N-path notch filters for the frequencies close to the switching frequency.

Moreover, from (3.7) and (3.8) the poles of $H_{0,SE}(f)$ and $H_{0,D}(f)$ for the single ended and the differential circuits are $s_{SE} = -2\pi D f_{rc,SE} + j2\pi k f_s$ and $s_D = -4\pi D f_{rc,D} + j2\pi(2k+1)f_s$ respectively. Where k=0, ±1, ±2, …. For k=0 we get the poles around f_s. Finally putting these poles equal to the poles of a parallel tank circuit we can find the following model parameters:

$$R_P = \frac{N\sin^2(\pi D) + D\pi^2(1-ND)}{N((D\pi)^2 - \sin^2(\pi D))} R_T = \frac{N^2\sin^2(\pi/N)}{\pi^2 - N^2\sin^2(\pi/N)} R_T\,|_{D=1/N},$$

$$C_P = \frac{ND\pi^2}{\zeta(N\sin^2(\pi D) + D\pi^2(1-ND))} C = \frac{\pi^2}{\zeta.N\sin^2(\pi/N)} C\,|_{D=1/N},$$

$$L_P = \frac{1}{(2\pi f_s)^2 C_P},$$

(3.10)

where ζ=2 for the single ended circuit and ζ=8 for the differential network; moreover, $R_T = R_S + R_L$. As you notice R_P and C_P are not frequency dependent which illustrates the fact that the bandwidth of the notch filter is not dependent to the

switching frequency and is fixed while the inductor L_P is changing with the switching frequency, determining the center frequency of the notch filter. In (3.10) the presence of "ζ" states that in the RLC model for the differential circuit the capacitance will be four times smaller than for the SE case, while L_P is four times larger. This means, with the same source and load resistances, Q for the differential case is four times smaller and the bandwidth will be four times larger. This is also intuitive since firstly for the differential circuit there are two series capacitors in each path and secondly each capacitor is exposed to the source and load resistors twice in each period which makes the effective resistance seen by the capacitors half compared to the single-ended version.

By applying the RLC model the main filter characteristics can be readily determined. As an example for an 8-path single-ended notch filter with N=8, $R_L = R_S = 50\,\Omega$ and C=7 pF we find:

$$R_P \approx 19(R_L + R_S) = 1.9\,k\Omega,$$

$$C_P \approx 4.2C = 29.4\,pF,$$

$$Notch\_Depth = 20\log(1 + R_P/(R_L + R_S)) = 26\,dB,$$

$$BW_{3dB} = \sqrt{(1 + R_P/(R_L + R_S))^2 - 2}\,/(2\pi R_P C_P) = 57\,MHz. \tag{3.11}$$

According to (3.11) notch depth is determined by the number of the paths which theoretically is limited to 26 dB for N=8. Increasing the number of paths will increase the depth of the notch.

3.4 Non-Idealities

3.4.1 Switch Resistance and Clock Rise and Fall Times

Switch resistance can readily be modeled in the RLC tank circuit as illustrated in Fig. 3.8 with R_{SW}. Moreover, the effect of rise and fall times can be approximated as a reduced duty-cycle in (3.3) and (3.4).

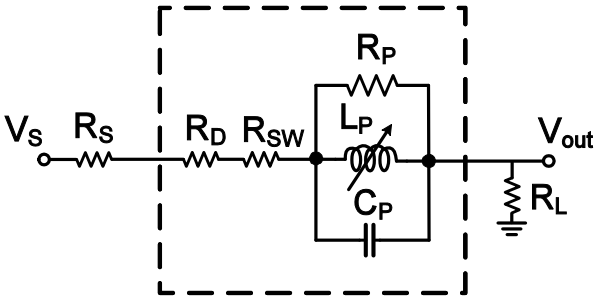

Figure 3.8. RLC model of the N-path notch filter including the effect of the switch resistance and the clock duty-cycle.

For the frequencies close to the switching frequency, the effect of the duty-cycle is already modeled in (3.9) and (3.10). The effect of reducing the duty-cycle on the pass-band can be extracted from (3.7) and (3.8), noting that the term (1-ND) becomes dominant in the pass band. To include the effects of the switch resistance and reduced duty-cycle we modify the model as shown in Fig. 3.8, where $R_D = (1-ND)(R_L + R_S + R_{SW})/(ND)$. Then the tank circuit should also be modified based on (3.10), substituting the actual D<(1/N) and $R_T = R_L + R_S + R_{SW}$. Consequently R_P will be increased.

Meanwhile changes of C_P and L_P are rather small. The consequence of extra resistance is increased insertion loss in the pass band, while the depth of the notch filter relative to the pass-band will also be increased. The transfer function for an 8-path notch filter and RLC model is illustrated in Fig. 3.9 for $R_{SW} = 6\,\Omega$ in case the duty-cycle is reduced by 15% compared to the ideal case (so 85% of 1/8). As can be seen, the insertion loss is increased by 2 dB and the depth of the notch by 3 dB.

3.4.2 Harmonic Mixing

So far the properties of the desired part in (3.2) which is represented as $V_{de}(f)$ in (3.3), have been discussed. In this section we explore the unwanted terms of (3.2) which are represented as $V_{un}(f)$ in (3.4). According to (3.4), $H_n(f)$ for n=±1, ±2, …, determines the possible unwanted terms.

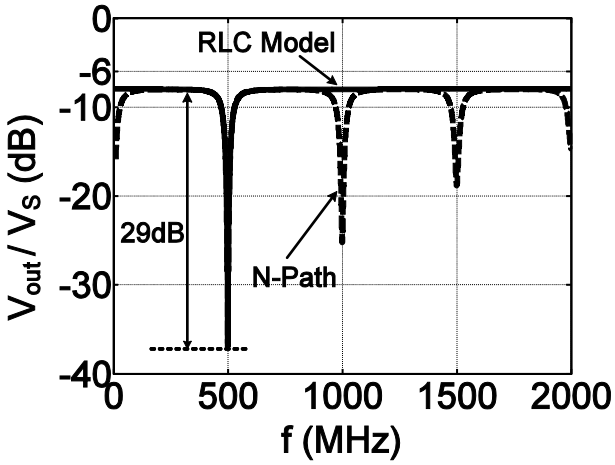

Figure 3.9. RLC model transfer function versus the N-path notch filter.

In (3.5) and (3.6) $H_{n,SE}(f)$ and $H_{n,D}(f)$ are non-zero for $n = kN$, where k=0, ±1, ±2, … and is zero for other values of "n". This implies that the unwanted terms will include folding from Nf_S+1 and Nf_S-1 due to $H_{\pm N}(f)$ and this will repeat for $H_{\pm 2N}(f)$, $H_{\pm 3N}(f)$, … .

Now as an example for an 8-path single-ended notch filter, from (3.4), (3.5) we define $H_{n,un,SE}(f) = (R_L/(R_L + R_S))H_{n,SE}(f)$ for n=8,16,24,… . $H_{n,un,D}(f)$ is represented for the differential architecture in the same way. $H_{n,un,SE}(f)$ and $H_{n,un,D}(f)$ determine the harmonic mixing coefficients in (3.4). In Fig. 3.10 for an 8-path single-ended and differential architecture $H_{n,un,SE}(f)$, $H_{n,un,D}(f)$ and also $V_{de}(f)/V_S(f)$ are shown. In Fig. 3.11 the desired term and the undesired term $H_{n,un,D}(f)$ is illustrated for n=8 and for the case the physical capacitor is increased as C=5, 10, 20 pF in each path. As we expect the amount of folding back components are decreased by increasing the capacitor. Accordingly similar to all N-path filters some time-invariant pre-filtering might be required in order to suppress unwanted folding terms sufficiently. Increasing the number of paths will move the aliasing components further away while increasing RC time constant also will decrease the unwanted terms which relax the requirements of the pre-filter.

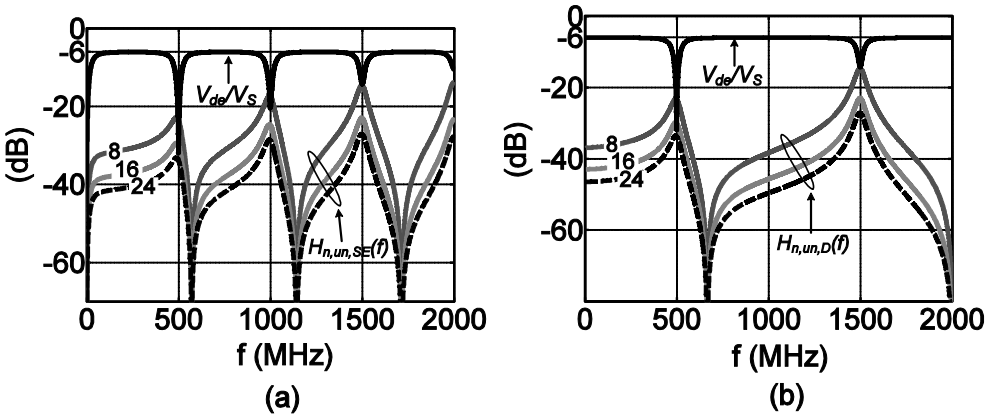

Figure 3.10. Desired (de) and unwanted folding back transfers $H_{n,un}$ for n=8,16,24 in: (a) a single-ended 8-path notch filter (b) a differential 8-path notch filter.

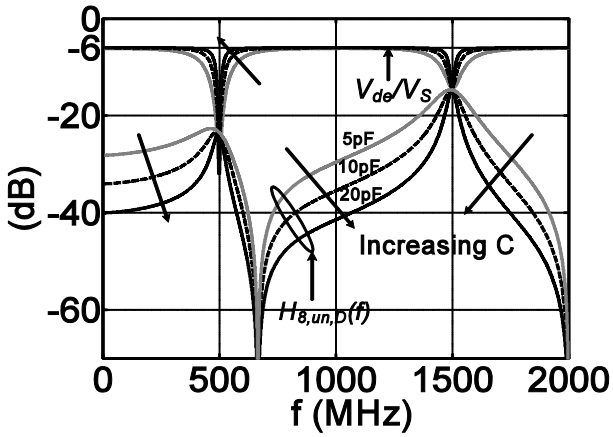

Figure 3.11. The effect of increasing "C" on the desired and undesired transfers of an N-path notch filter.

3.4.3 Noise Analysis

If the switches in Fig. 3.3 and the driving clock phases are ideal, neglecting the noise of R_L then all the noise which appears at the output originates from the input resistance R_S. In the pass-band the transfer function for the noise of R_S which goes to the output, similar to the desired input signal, complies with (3.2) which includes the direct transfer and folding of uncorrelated noise power from higher harmonics.

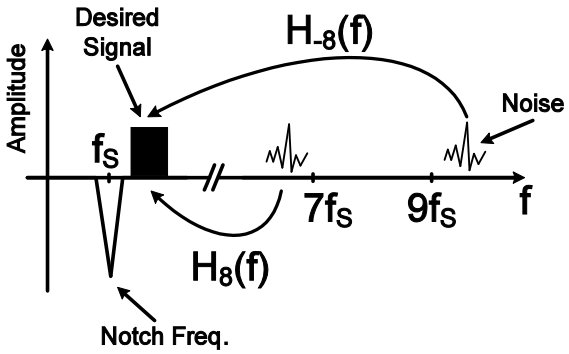

Figure 3.12. Noise folding in an 8-path notch filter.

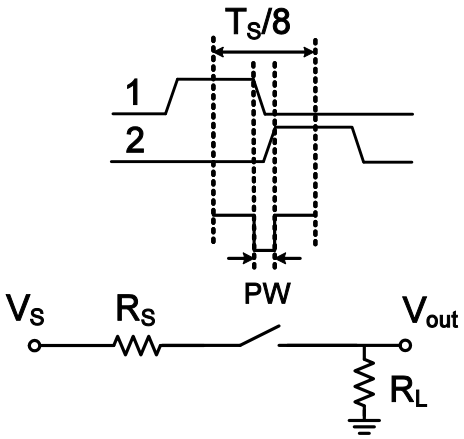

Figure 3.13. Modeling of clock rise/fall times as a mixer.

As an example two folding components that occur in an 8-path system with $H_{\pm 8}(f)$ are shown in Fig. 3.12. As a result the output noise can be readily calculated from (3.2). For an 8-path notch filter shown in Fig. 3.10 the folding back components are negligible and simulation and calculation from (3.2) renders a noise figure of NF<0.1 dB for an ideal 8-path filter. If we include the non-idealities of the switch resistance and the reduced duty-cycle, NF will degrade. If the duty-cycle is smaller than 1/N then the circuit behavior in the pass-band can be modeled as in Fig. 3.13. The tank circuit is modeled as a short circuit and the reduced duty-cycle is modeled as a switch (mixer) which is on except for the clock overlap time of PW=(1-ND)T_s. This mixer will cause extra noise folding and also increased insertion loss in the

pass-band. The noise at the output can be found by calculating the Fourier series coefficients as:

$$N_{out} = \left((\frac{R_L}{R_T} ND)^2 + \sum_{n=1}^{+\infty} \left(-\frac{R_L}{R_T} \frac{2}{n\pi} \sin(n\pi(1-ND)) \right)^2 \right) (4kT(R_S + R_{SW}), \qquad (3.12)$$

where $R_T = R_L + R_S + R_{SW}$. Finally, the noise factor can be calculated as $F = N_{out}/(A_v^2 N_{in})$, where $N_{in} = 4kTR_S$. As an example for an 8-path single-ended notch filter if we assume $R_{SW} = 5\,\Omega$ and 15% reduction compared to the 1/8 duty-cycle, we find NF=1.7 dB and an insertion loss in the pass band of 2.2 dB. As a rough rule of thumb practical values of the noise figure are close to the insertion loss in dB.

3.4.4 Mismatch and Phase Imbalance

As discussed in section 3.4.2 a nice property of an N-path system is that many unwanted terms in $H_n(f)$ are canceled. As we derived in (3.5) and (3.6), this is due to the fact that different paths in an N-path system have equal amplitude responses but different phase shifts such that the vectorial summation is zero. In case there is any mismatch between different paths or phase imbalance in multiphase clocks, the cancellation becomes imperfect so that unwanted terms come up. We can quantify this effect with the derivations in (3.5) and (3.6). As an example we consider an 8-path single-ended system with a phase imbalance in the clock. Suppose one of the clock phases has a different duty-cycle from other paths. Then as shown in Fig. 3.14 the first harmonic of $H_1(f)$ which is cancelled in the ideal case is showing itself as an undesired term. The strength of the unwanted transfer curves are related to the amount of mismatch.

3.5 Implementation of 8-Path Notch Filters

Both a prototype of the SE and differential notch filter were implemented in a 65 nm CMOS technology. The schematic is shown in Fig. 3.15 and a chip photo in Fig. 3.16. The switches are realized by low threshold NMOS transistors and the capacitors with MIM technology.

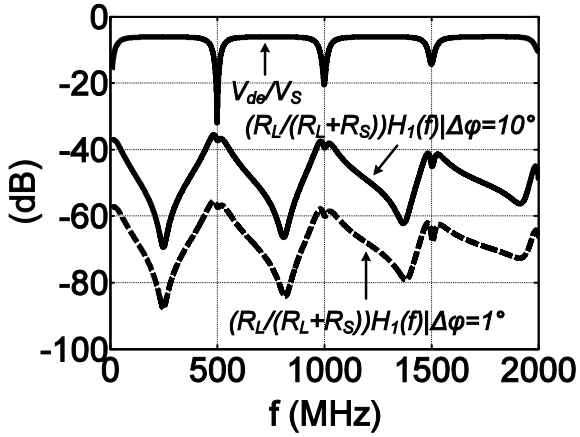

Figure 3.14. The effect of phase imbalance on the N-path notch filter desired and undesired transfers.

Large switch sizes (W/L=100u/65 nm) are used resulting in a switch resistance of 6 Ω when driven by a swing of 0.9 V (the DC voltage on the source/drains of the switches is set to 300 mV to avoid reliability issues at high input swings). The linearity of the N-path notch filters is mainly determined by the linearity of the NMOS switches and the capacitors. Apart from reducing the switch resistance, applying a large switch size will improve the linearity of the filter as well. Moreover, MIM capacitors have better linearity compared to CMOS capacitors with a comparable capacitance density. Thus a very high linearity for the N-path notch filters is achievable in the new CMOS technologies. Larger switches would increase the insertion loss at high frequencies due to the parasitic capacitance at the RF-nodes and would require higher digital drive power. In the SE filter C=7 pF is chosen in each path targeting to suppress a blocker with 6 MHz bandwidth (e.g. a strong TV channel which blocks a Cognitive Radio receiver exploiting TV white spaces as allowed by the FCC [16]). For the differential architecture 32 NMOS transistors are realizing the left and right mixers in Fig. 3.15. Two capacitors are in series and in order to get the same RC product as the SE version we have doubled the capacitor value (C=14 pF). Please note that for the differential architecture in the measurement setup the (differential) source and load resistors are 100 Ω while it is 50 Ω in the SE notch filter. As a result the factor of four in the Q reduction in compare with the single-ended filter as we discussed in section 3.3.2 is compensated by doubling the capacitor size and source and load resistors for the differential architecture.

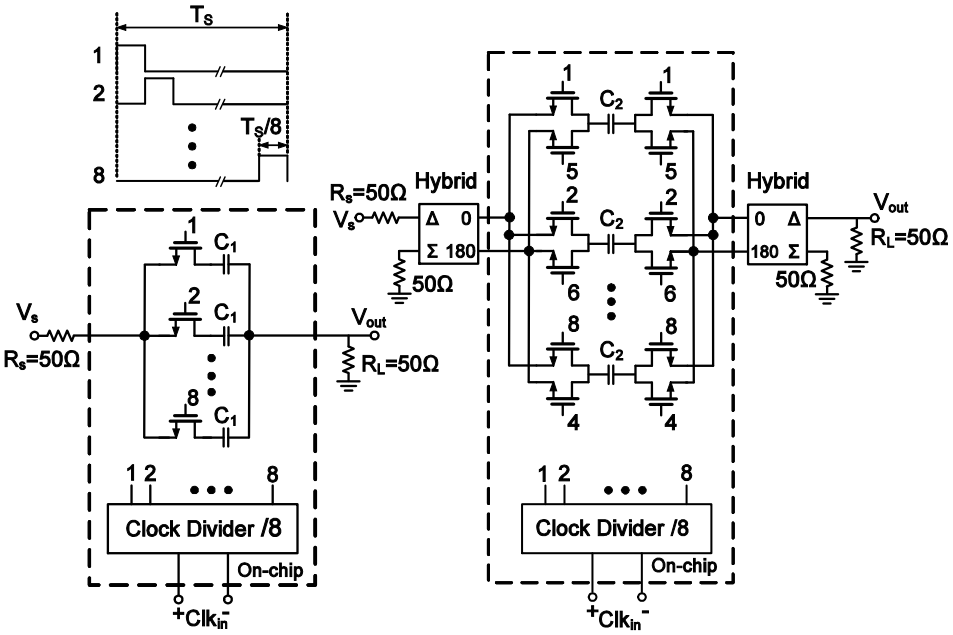

Figure 3.15. An 8-path single ended and a differential notch filters.

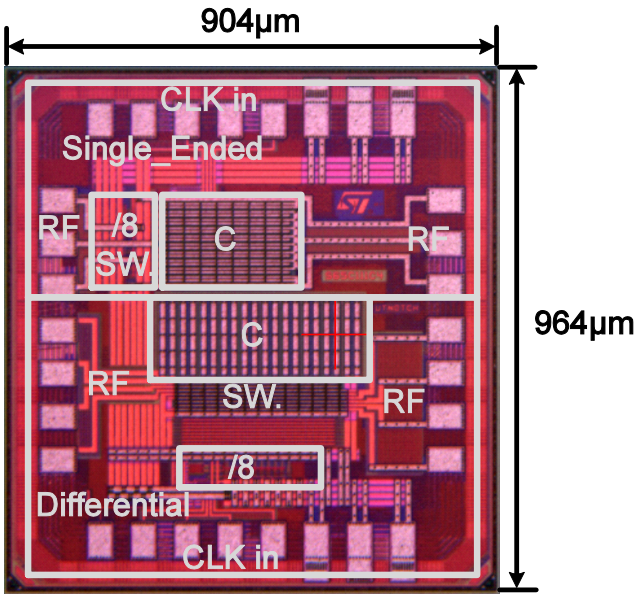

Figure 3.16. Chip micrograph in 65nm CMOS technology.

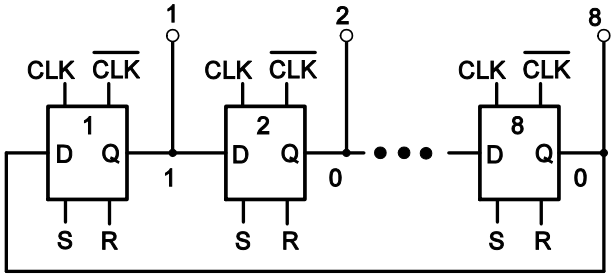

Figure 3.17. A divide by 8 ring counter.

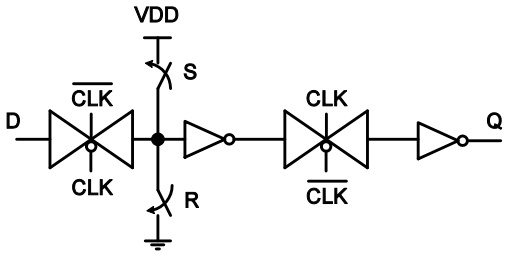

Figure 3.18. Transmission gate D flip-flop used in the ring counter.

As shown in Fig. 3.16 both the input and the output switches for the differential architecture are placed in one side of the capacitors to facilitate the routing of the 8-phase clock to 32 switches in the layout avoiding resistive and capacitive mismatch. Moreover, in order to provide enough isolation between switches, they are realized inside separate deep N-wells. For each filter, a divide-by-8 ring counter is implemented to provide a proper phase balance. The divider is composed of 8 transmission gate flip-flops in a ring (see Fig. 3.17 and 3.18).

During startup the output of the first flip-flop is set to VDD and the outputs of the other flip-flops are set to ground. Then a clock activates the ring divider and at the output of the 8 flip-flops multiphase clocks with 1/8 duty-cycle and with the frequency of 1/8 of the clock frequency are generated. This architecture inherently has a good phase performance since just the rising edge of the clock is used. Moreover, different phases are directly generated in the ring without applying any extra logic circuits which might add errors to the multiphase clocks. The input frequency range of the clock divider is 0.8-9.6 GHz. The generated phases in the divider are buffered and fed to the switches.

3.6 Measurement Results and Comparison

Measurement results of the main characteristics of the SE and the differential notch filters are shown in Fig. 3.19 and 3.20 respectively for f_s at 500 MHz. The maximum depth of the notch filters is limited to 24 dB for $f_s = 500\ MHz$ while it is reduced to 21 dB as the switching frequency increased. Remember the theoretical value of the maximum rejection for an ideal 8-path filter as calculated in section 3.3 is 26 dB. The deviation between the measured and calculated rejection at f_s is due to the charge injection in the switches and small charge sharing between different capacitors at high frequencies. S_{21} renders 1.4-2.5 dB insertion loss in the pass-band in the SE filter. The amount of insertion loss for the differential filter is 1.4-2.8 dB in the pass-band. At $f_s = 500\ MHz$ according to the simulation results, the rise and fall times of the clock phases driving the switches are approximately 18 ps which presents approximately 15% of the pulse width ($T_s / 8 = 250\ ps$).

As we showed through an example in section 3.4.1 and in Fig. 3.9 with 15% reduction in the duty-cycle and the on resistance of 6 Ω for NMOS switches, in the RLC model the insertion loss is 2 dB. Please note 15% of duty-cycle reduction in this case is quite pessimistic since the NMOS switches even during the rise and fall times are conducting. By increasing the switching frequency the rise and fall times of the multiphase clocks consist a significant portion of the pulse width which result in reduced the effective duty-cycle and consequently increased insertion loss.

Power matching is provided in the pass-band for both filters. As expected the incident signal is reflected at the switching frequency and passes through for other bands except the harmonics of the switching frequency. The corner frequencies for S_{11}<-10 dB are also shown in Fig. 3.19 and 3.20. The measured IIP3 is better than +17 dBm and P_{1dB} is between 2-6 dBm. P_{1dB} in the pass-band is measured as -3 dBm when a blocker with a power of 0 dBm is applied at f_s. The NF, measured in the pass-band is 1.2-2.8 for the SE and 1.6-2.5 dB for the differential filter for the switching frequencies of 0.1-1.2 GHz which is roughly the same as the loss in dB. NF increases at the notch frequency due to the fact that the signal is attenuated around the switching frequency, while the noise from the switch resistance and also folded back noise from higher harmonics still can appear at the output. For the differential filter as we expect there is no rejection at the second harmonic.

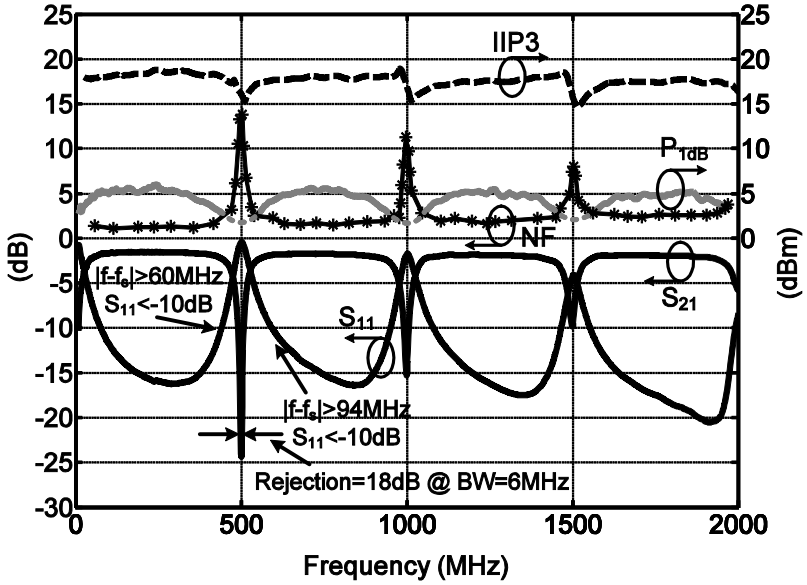

Figure 3.19. S_{21}, S_{11}, NF, P_{1dB} and IIP3 of the single-ended notch filter.

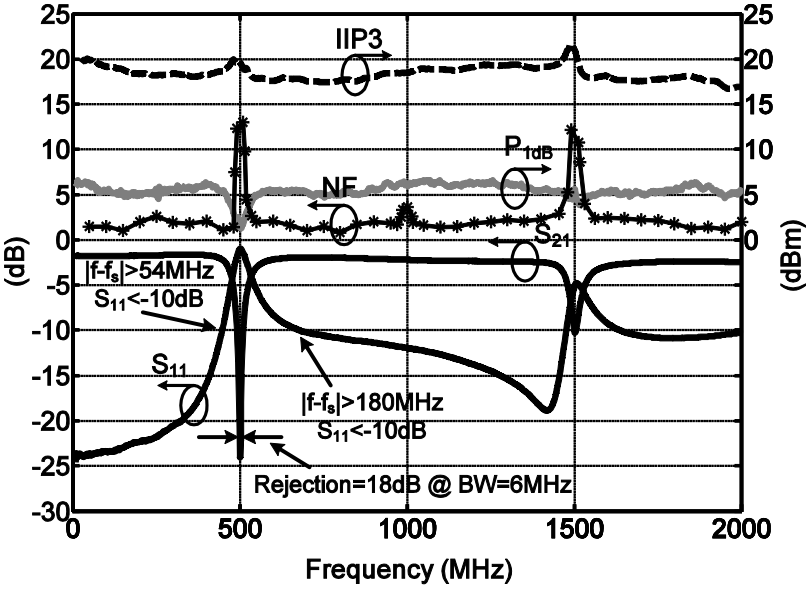

Figure 3.20. S_{21}, S_{11}, NF, P_{1dB} and IIP3 of the differential notch filter.

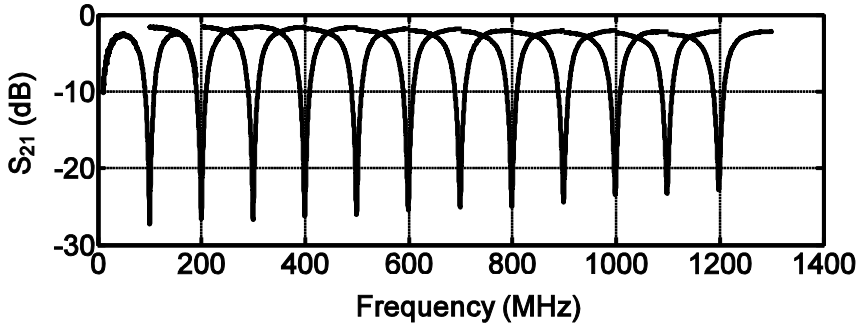

Figure 3.21. S_{21} in the single-ended filter for the switching frequency of f_s=0.1-1.2 GHz.

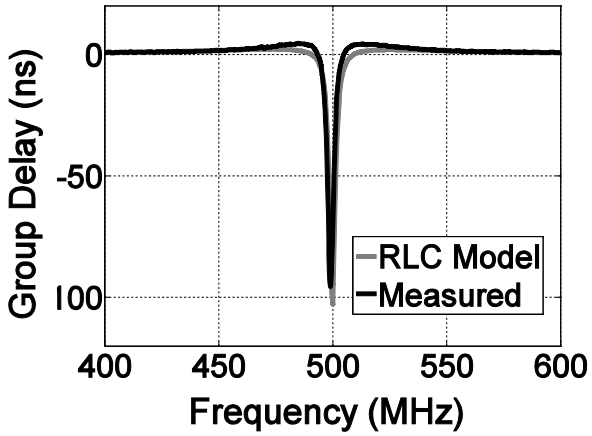

Figure 3.22. Measured group delay of the single-ended notch filter compared with the RLC model at f_s=500 MHz.

The increased noise figure around the second harmonic in this case is due to the leakage of the second harmonic of the clock. The tunability of the filter is illustrated in Fig. 3.21, showing S_{21} of the SE filter for $f_s = 0.1-1.2\,GHz$. The differential filter shows the same behavior.

The group delay of the SE filter is measured and shown in Fig. 3.22 and compared to the prediction by the RLC model in Fig. 3.8. Similar to a passive tank circuit the group delay becomes flat in the pass-band representing a linear phase operation.

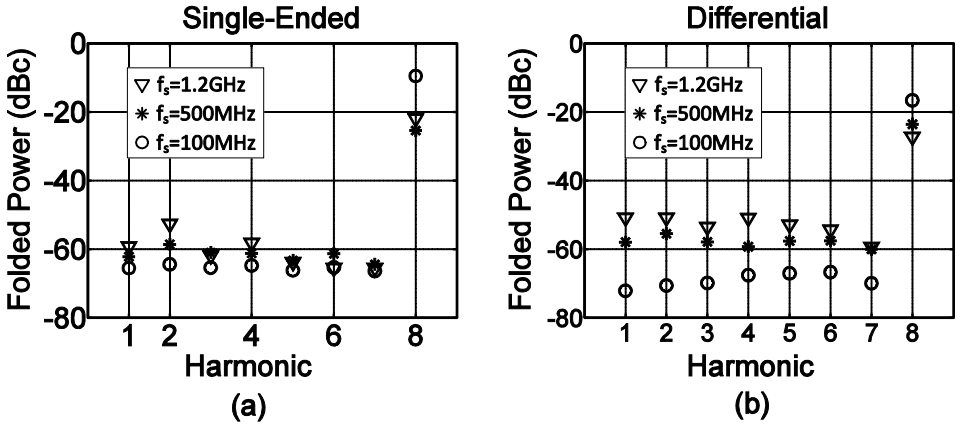

Figure 3.23. Measured harmonic mixing of 10 samples for (a) single-ended (b) differential notch filters.

In order to check the effect of the phase imbalance and mismatch on the performance of the filter we have measured the harmonic mixing effect in 10 samples for 3 switching frequencies in the SE and differential notch filters. Fig. 3.23 illustrates the worst-case numbers of harmonic mixing in the pass-band. We also tried to measure the noise figure in the pass-band, under blocking conditions. In simulation we found that by applying a blocker of -5 dBm at f_S, the NF in the pass-band degrades by 1 dB. Due to the noise floor of our signal generator we didn't manage to measure this directly.The maximum rejection of the filters is measured with the existence of a blocker at the notch frequency (see Fig. 3.24). The amount of rejection is degraded by increasing the blocker power, but this only happens at high blocker power levels. Interesting differences are observed here between the SE and differential filter. The SE filter input port might be chosen at the capacitor side (left in Fig. 3.15), but also at the switching side (right side). As it is shown in Fig. 3.24 choosing the switching side as the input port is better in terms of notch depth under strong blocking conditions (the rejection degrades starting at -3 dBm versus -8 dBm). The reason for the degradation of the notch depth is charge leakage from the capacitors with the existence of the large input power. Note that the DC level on the drain/source of the switches is 300 mV. If the input swing is larger than 300 mV then the voltage on the source/drain of the switches might become negative and as a result some of switches which are supposed to be off with zero gate voltage, start to conduct and unwanted charge leakage happens which reduces the amount of the maximum rejection at notch frequency.

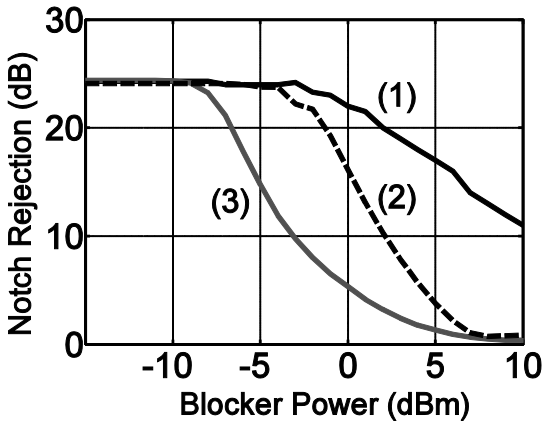

Figure 3.24. Measured maximum rejection of notch filters with a blocker at notch frequency: Case 1- The differential notch filter. Case 2-The single-ended notch filter when the input is the switching side of the filter. Case 3- The single-ended notch filter when the input is the capacitor side of the filter.

Now assume that in the SE filter we apply a sinusoidal signal with the frequency of the switching frequency to the capacitor side. The voltages over the capacitors will have a constant value. This voltage is in fact the average of the portion of the signal which is seen by each capacitor periodically. As a result the voltage on the drain/source of the switches will be the input signal with a shifted DC level which can be negative also for the negative parts of the input signal. Then the voltage on the source/drain of the switches might be even more negative which results in severe charge leakage compared to the case of choosing the switching side as the input. Although the differential filter is reciprocal for small signals, this may change at large signals. Unlike the input set of switches, the set of the switches at the output will not experience a large swing with the existence of a large blocker at the input. As a result the charge leakage from the capacitors will be limited and consequently the blocker performance of the differential notch filter is significantly better than the single-ended version. The measured clock leakage at the input port for the SE and the differential filter is better than -75 dBm and -60 dBm respectively at the switching frequency. These values are lower than -57 dBm spurious domain emission limit for frequencies lower than 1 GHz, as specified by FCC part 15 [21]. The larger LO leakage in the differential architecture is mainly due to the larger overlap between input/output lines and the clock lines in the layout for the differential filter.

To put these results in perspective, the key measured parameters of both filters are compared with results of two Q-enhanced notch filters [22, 23]. Compared to the Q-enhancement techniques a much larger tuning range with higher dynamic range is achievable with the N-path technique. Also, Q-enhanced notch filters cannot handle large blockers: the maximum rejection of 44 dB reduces to 3 dB with a blocker level of -5 dBm while the implemented 8-path notch filters still provide their default 24 dB of rejection with the existence of -5 dBm blocker level. The center frequency is determined with the clock frequency which is very robust while in the LC resonator based architectures the sensitivity of the center frequency to PVT variations is significant. Moreover the die area is much smaller, especially at low GHz bands.

Table 3.1. Comparison With Other Designs.

	Differential	Single-Ended	[22]	[23]
Technology	CMOS 65 nm	CMOS 65 nm	CMOS 0.13 um	CMOS 0.18 um
Active Area	0.14 mm^2	0.07 mm^2	1.6 $mm^{2(1)}$	0.51 $mm^{2(1)}$
Tuning Range	0.1-1.2 GHz	0.1-1.2 GHz	4.7-5.4 GHz	5.4-6 GHz
Max. Rejection	21 to 24 dB	21 to 24 dB	44 dB	35.7 dB
Max. Rejection with -5dBm Blocker @ Notch Freq.	24 dB @ f_s=500 MHz	24 dB @ f_s=500 MHz	3 dB	NA
Rejection	18 dB @ 6 MHz	18 dB @ 6 MHz	10 dB @ 20 MHz	NA
Pass-Band Gain	-1.4 to -2.8 dB	-1.4 to -2.5 dB	19.4 $dB^{(1)}$	14.7 $dB^{(1)}$
NF (dB)	1.6 to 2.5 dB	1.2-2.8 dB	3.5 $dB^{(1)}$	5.3 $dB^{(1)}$
P_{1dB} (dBm)	6	2-6	$-9.4^{(1)}$	NA
IIP3 (dBm)	>17	>18	$-2.9^{(1)}$	$-2.5^{(1)}$
LO Leakage (dBm)	<-60	<-75	-	-
Power Consumption	3.5 to 30 mW @ (0.1 -1.2 GHz)	2 to 16 mW @(0.1-1.2 GHz)	7.5 mW	1.8 mW

(1) A notch filter with an LNA are included in the reported numbers.

3.7 Conclusions

Widely tunable filters with good linearity and blocking performance are very much wanted to address blocking issues in both multi-mode wireless transceiver systems co-existing on a single chip as well as software-defined and cognitive radio systems. In this context N-path filtering seems quite promising, as it provides digital programmability of the center frequency via a digital clock frequency with a small sensitivity to the PVT variations, offers good linearity and compression performance by using passive mixers with capacitors driven by digital clock, which all fit nicely to CMOS technology scaling. This chapter discusses N-path notch filter circuits and models their performance, quantifying both transfer properties and several important non-idealities. The filter performance is verified for both a single ended and differential notch filter in 65nm CMOS, digitally tunable over more than a decade from 100 MHz-1.2 GHz. Measured filter transfer and noise properties fit well to theory, showing 1.2-2.8 conversion loss in the pass-band, and a rejection in the notch which is always >18 dB over 6 MHz bandwidth over the entire tuning range. Unwanted folding is present, but up to the 8th harmonic, rejection is better than -50 dBc. Linearity is consistently high (IIP3>17 dBm) and compression points well above 0 dBm are achievable. Compared to Q-enhanced LC filters with similar Q-value, the filter maintains shape up to much higher blocking levels.

3.8 References

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Chapter 4

A 4-Element Phased-Array System with Simultaneous Spatial- and Frequency-Domain Filtering at the Antenna Inputs

4.1 Introduction

The abundance of wireless communication devices in the low GHz frequency bands results in potentially strong mutual interference between devices, often referred to as “blocking”. Blocking signals can exist both in-band and out-of-band, where especially the requirements on the latter tend to be strong. The GSM and Bluetooth standards for instance specify 0 dBm out-of-band blockers. Note that 0 dBm received power in a 50 Ω impedance corresponds to a voltage swing of 0.6 Vpp, which is difficult to handle by CMOS circuits with a supply voltage of around 1Volt! When mobile devices are in close proximity, blockers even stronger than 0 dBm may occur, not only out-of-band but also in-band.

Such in-band interference scenarios[1] are also an important bottleneck for future dynamic spectrum access via a cognitive radio, where unused spectrum may exist in close spectral proximity to strong signals. In order to reduce the out-of-band blockers, RF bandpass pre-filtering is commonly used. However, such frequency-domain filtering does not help for in-band blocking. Spatial filtering through a phased-array antenna can reduce blockers, both out-of-band and in-band. In a phased-array, in-beam phase shifted signals from multiple antennas add constructively, while out-of-beam signals add destructively.

To align in-beam phase-shifted signals, different approaches have been presented in literature. Among them, passive RF phase-shifting in the signal path is attractive from a linearity point of view. However, passive RF components tend to take a large die area and their loss results in signal attenuation and noise figure degradation [1, 2]. In the low GHz frequency range, the LO phase shifting and vector modulation techniques which do not need on-chip inductors for phase shifting gained interest in recent years [3-6]. Array size consideration often dictate a limited number of antenna elements, so that all phase shifted signals can be summed, usually at a summation point after some active blocks, providing amplification and sometimes frequency downconversion. Thus the interfering signals are amplified before they are canceled at the summation point. This requires a high dynamic range for the blocks preceding the summing node to handle the strong blocking signals. A fully passive switched-capacitor approach is presented in [6] to improve the input referred compression point of the phased-array receiver, providing P_{1dB}=+2 dBm, but at a high noise penalty (NF=18 dB).

This chapter discusses a mixer-first phased-array receiver that combines beamforming and N-path filtering [7]. It achieves up to +10 dBm out-of-band/beam[2] compression point and 3-6 dB single element noise figure. This chapter elaborates on the phased-array system and includes a comprehensive mathematical analysis of the Spatial- and frequency-domain filtering at the antenna inputs and also at the baseband. Simulation and measurement results are provided together with a comparison to analytical results.

[1] Actually the difference between in-band and out-of-band is blurred for cognitive radio scenarios exploiting white spaces (there is no clear dedicated band but just used/unused spectrum).

[2] Two measurement cases are considered here: (1) In-beam and out-of-band (2) In-band and out-of-beam blockers.

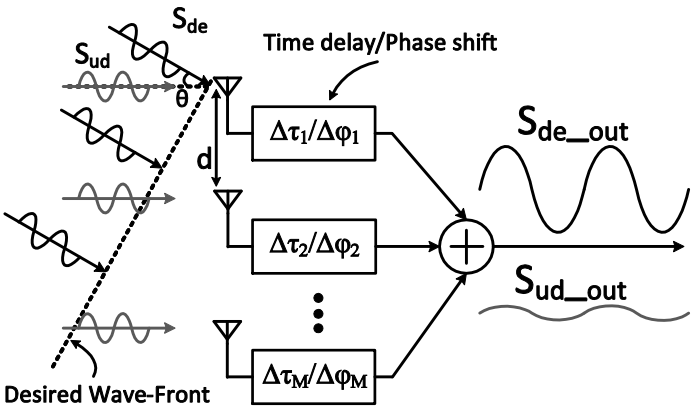

Figure 4.1. A general block diagram of an M-element phased-array antenna system. θ is the angle between the incident signal and the normal line to the antenna axis.

In section 4.2 a brief summary of a phased-array system is presented. The mixer-first phased-array system is discussed intuitively in section 4.3. The mathematical analysis of the proposed system is presented in section 4.4. The implemented prototype will be discussed in section 4.5. Section 4.6 discusses the analysis implications on the implemented architecture. and finally the measurement results are presented in section 4.7.

4.2 Multi-Antenna Phased-Array System

A general block diagram of an M-element linear phased-array antenna system is illustrated in Fig. 4.1. The desired planar wave signal (S_{de}) is incident on the antennas at an angle θ to broadside, while an undesired signal (S_{ud}) also hits the receiver antennas with a different spatial angle from the desired signal. Depending on the spatial angle θ, these signals experience different travel times to reach different antennas. This causes a time delay on the signals reaching two neighbor antennas which can be calculated as:

$$\Delta\tau = d.\sin(\theta)/c, \tag{4.1}$$

where "*c*" is the speed of light and "*d*" is the physical distance between antennas. The time delay in the desired signals should be compensated via true time delay blocks or phase shifters in the receiver before summation point (see Fig. 4.1). The modulated signal arriving at the first (upper) antenna in Fig. 4.1 can be written as

$s_{in,1}(t) = \mathrm{Re}\{A(t)e^{j\omega_c t}\}$ in which $A(t) = |A(t)|e^{j\varphi(t)}$ is the baseband modulating signal. As a result the input signal at the first antenna is: $s_{in,1}(t) = |A(t)|\cos(\omega_c t + \varphi(t))$, and in general the received signal at mth antenna (m=1,2,…) experience delay of $(m-1)\Delta\tau$:

$$s_{in,m}(t) = s_{in,1}(t-(m-1)\Delta\tau) = \left|\mathrm{A(t-(m-1)}\Delta\tau\right|\cos(\omega_c t - \omega_c(m-1)\Delta\tau + \varphi(t-(m-1)\Delta\tau)). \quad (4.2)$$

Generally speaking the time delay in (4.2) should be compensated via true time delay blocks before the summation point in Fig. 4.1 to align the received signals for a desired direction of reception. However, for narrow band systems where $BW << \omega_c$ an approximation can be made to replace true time delay with phase shifting blocks. To understand this, note that in a phased-array system the physical distance between antennas (d) is usually chosen as large as possible to realize narrow beam patterns. In order to avoid grating lobes [8] the distance between antenna elements should be ($d \leq \lambda_{min}/2$) where λ_{min} is the minimum wavelength of the received signal. Assuming a narrow band system and $d = \lambda_c/2$ in which λ_c is the wavelength of the carrier frequency, the delay time in (4.1) becomes very small compared to the changes of the baseband signal. As a result, the approximations $A(t-(m-1)\Delta\tau) \approx A(t)$ and $\varphi(t-(m-1)\Delta\tau) \approx \varphi(t)$ can be applied. Consequently (4.2) for a narrowband case can be rewritten as:

$$s_{in,m}(t) \approx \left|\mathrm{A(t)}\right|\cos(\omega_c t - \omega_c(m-1)\Delta\tau + \varphi(t)). \quad (4.3)$$

Considering (4.3) now the fixed phase shift of $\Delta\varphi_m = -\omega_c(m-1)\Delta\tau$ should be compensated. This can be easily done for instance by applying a phase-shifted clock in the LO path of a mixer. If the time delay is compensated for the desired angle of reception (in-beam signals) the beams add-up constructively while for out-of-beam signals add destructively. Thus providing spatial filtering for different beams [9]. Phase shifting instead of true time delay causes an artifact so called beam squinting (i.e. frequency dependent beam direction). For narrow band applications this effect can be neglected [10]. More than spatial filtering a phased-array system has a benefit of signal to noise ratio (SNR) improvement, compared to a single antenna receiver. In fact for every doubling of the receivers in a multi-antenna systems presented in Fig. 4.1, the sensitivity is improved by 3 dB theoretically at the cost of doubling both effective antenna area and receiver power consumption.

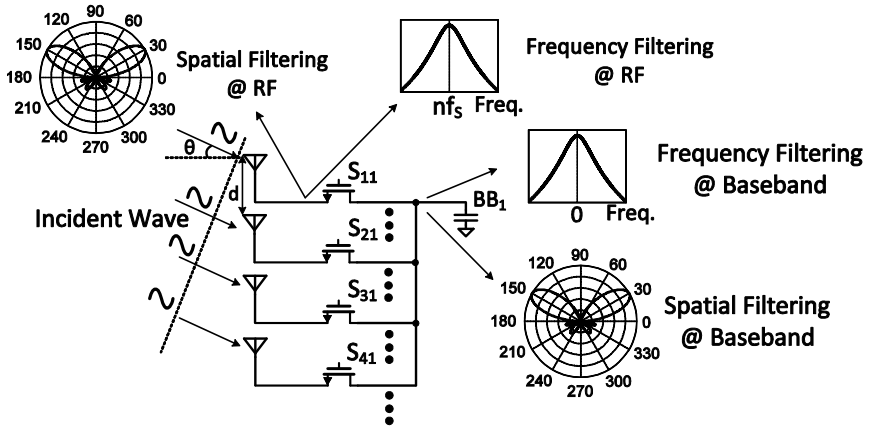

Figure 4.2. Spatial- and frequency-domain filtering in a mixer-first phased-array system for θ=30°.

Assuming uncorrelated noise in different receive paths, noise signals add up in power while the desired signals are correlated and add up in voltage gaining a factor of two in SNR, i.e. 3 dB improvement.

4.3 Mixer-First Phased-Array Architecture

4.3.1 Spatial- and Frequency-Domain Filtering

In this section the phased-array receiver in which the Spatial- and frequency domain filtering occurs at the antenna inputs, is discussed intuitively. A simplified block diagram of a mixer-first 4-element phased-array receiver is illustrated in Fig. 4.2. The received signal at the antenna inputs is directly downconverted on the baseband capacitors via multiphase passive mixers, driven by non-overlapping clocks.

The phase shift of the RF signals can be compensated by LO phase shifting in the mixers. If the RC time constant composed of the real impedance of the antennas and the baseband capacitors is large enough compared to the on-time of the mixer switches, the downconverted signals for the desired incident angle after alignment in phase is summed on the baseband capacitors constructively.

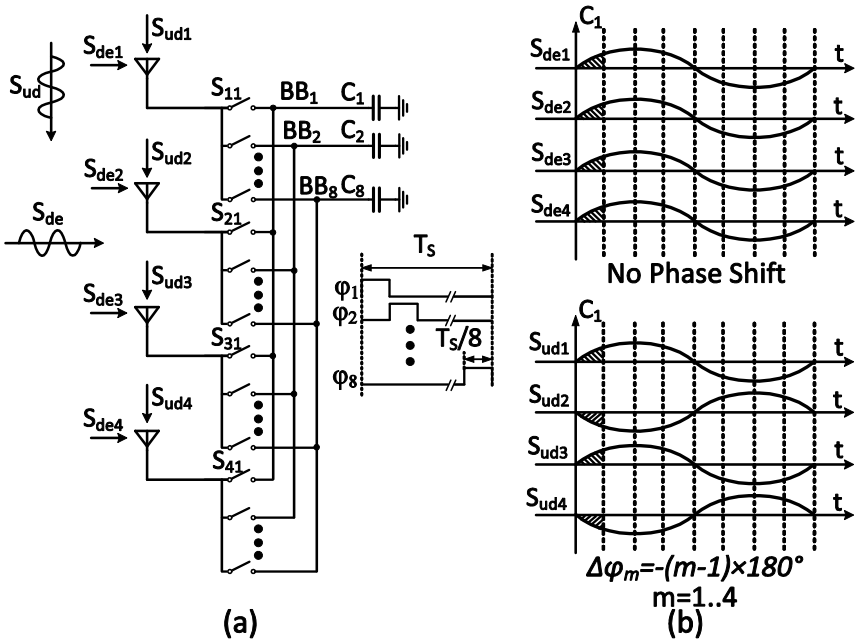

Figure 4.3. (a) Mixer first 4-element phased-array system (b) Timing diagram for desired signal (S_{de}) and undesired signal (S_{ud}) incident to the antennas at 0 and 90 degrees respectively.

For out-of-beam signals the summation would be partly or fully destructive, thus resulting a spatial filtering on the baseband capacitors (see beam pattern @baseband in Fig. 4.2). This spatial filtering is upconverted to the RF node via passive mixers, so that it occurs directly at the antenna inputs. Moreover RC low-pass filtering also occurs on the capacitors, which is also upconverted rendering high-Q N-path frequency-domain filtering at RF [11, 12].

In order to understand the spatial filtering intuitively a 4-element phased-array system with 8-phase passive mixers is examined in Fig. 4.3 for two different incident angles. The passive mixers are driven by 8 non-overlapping 1/8 duty-cycle clocks (φ_1-φ_8). For simplicity we assumed in the architecture of Fig. 4.3 all switches connected to the same capacitors are driven with the same clock phases thus realizing zero angle reception. By selecting other clock phases for the mixer switches, beam steering can be achieved for 8 discrete possible angles.

In Fig. 4.3 the desired signal (S_{de}) with the frequency of the switching frequency (f_S) is impinging the receiver antennas with a zero spatial angle (θ=0°) while the

undesired signal (S_{ud}) is arriving at the antennas with θ=90°. The time domain signals are illustrated in Fig. 4.3b for the two incident angels. Note that for desired signal there is no time delay among received signals while for the incident angle of θ=90°, assuming d= $\lambda_c/2$ the phase shift can be calculated from (4.1)-(4.3) as:

$$\Delta\varphi_m = -\omega_c(m-1)\Delta\tau = -(m-1)\pi\sin(\theta). \tag{4.4}$$

As a result for θ=90°, the phase shift for m^{th} antenna will be $\Delta\varphi_m = -(m-1)\times 180°$ (m=1, 2 ,3 ,4). This phase shift is illustrated for the undesired signal (S_{ud}) in Fig. 4.3b. In Fig. 4.3b parts of the signals which are seen by the capacitor C_1 are shown as shaded area. Please note that for the desired angle of reception capacitor C_1 sees the same parts of the signal periodically which will be integrated on the capacitor. However; for the undesired signal, capacitor C_1 is exposed to the anti-phase signals successively which will be canceled out if the RC time constant is large enough. This illustrates spatial filtering on the baseband capacitors. As a passive mixer periodically acts as a transparent switch, this filtering is also seen at the antenna node before the switches. In fact for the undesired direction of the incident wave, the receiver input roughly acts as a short circuit to each antenna, reflecting the undesired signal. Note that this is not the case for an active mixer, which ideally acts uni-lateral from input to output and has reverse isolation.

Considering a single element in Fig. 4.3, an N-path RC frequency-domain filtering also occurs on the baseband capacitors which is upconverted to the switching frequency and its harmonics [13-15]. This is due to the periodically time-variant nature of N-path filters, which introduces frequency shifts by multiples of the clock frequency. Thus the Spatial- and frequency-domain filtering happens not only around the fundamental harmonic of the clock but also around its harmonics. In this work we will aim at 3^{rd} harmonic reception, as it allows for an increase in frequency range, whereas the power efficiency is also higher compared to fundamental reception. Moreover, it significantly reduces the chip area for high frequency clock distribution.

4.3.2 Spatial Angular Resolution

As mentioned in the previous section the phase of the LO controls beam direction. Thus the spatial angle resolution is defined by the number of different mixer clock phases. In our design [6] we used 8-phase passive mixers so that the

possible electrical phase shifts are $\Delta\varphi = 0°, \pm 45°, \pm 90°, \pm 135°, 180°$. By applying (4.4), we can find the following corresponding spatial angles: $\theta = 0°, \pm 14.48°, \pm 30°, \pm 48.6°, 90°$.

4.4 Analysis

In this section we will provide a set of closed form equations to describe the Spatial- and frequency domain filtering of the mixer-first phased-array system discussed in previous section. The mathematical equations will illustrate the Spatial- and frequency domain filtering both on the baseband capacitors and at the antenna terminal. The network of Fig. 4.3 is a switched-RC Linear Periodically Time Variant (LPTV) network. R_S mimics the real part of the antenna impedance (50 Ω) The analysis of single state switched-RC networks where the capacitor voltages do not have any interaction with each other (non-overlapping clocks), is extensively discussed in [13, 16]. Here to avoid tedious mathematical derivations we will just mention the assumptions and provide the final results of the mathematical modeling. The analysis will cover two cases of zero degrees and also -30 degrees for reception angle of the main beam. The analysis for other angles can be derived similarly.

All of the analysis results in the following sections are cross-checked with simulation results from Spectre-RF with ideal switches. Since the simulation results fall exactly on top of the analyzed ones we have omitted the simulation results.

4.4.1 Baseband Analysis at Zero Incident Angle

Since we have assumed that there is no overlap between multiphase clocks which drive the mixer switches, there is no cross-talk between baseband capacitors. As a result the analysis of the switched-RC network of Fig. 4.3 in a general form with N-phase passive mixer and 4 receiver elements can be simplified to the analysis of the network illustrated in Fig. 4.4a which includes only a single baseband capacitor. The transfer for the other capacitors can be found as phase-shifted versions of the analyzed one. In Fig. 4.4a only the switches which are connected to a single capacitor are shown. The LPTV analysis can be carried out for all “N” possible LO phase settings. “N” is the number of the paths in the passive mixer (in our case N=8). In this section we will provide the equations for zero-angle spatial reception, in this case all switches in Fig. 4.4a are in phase.

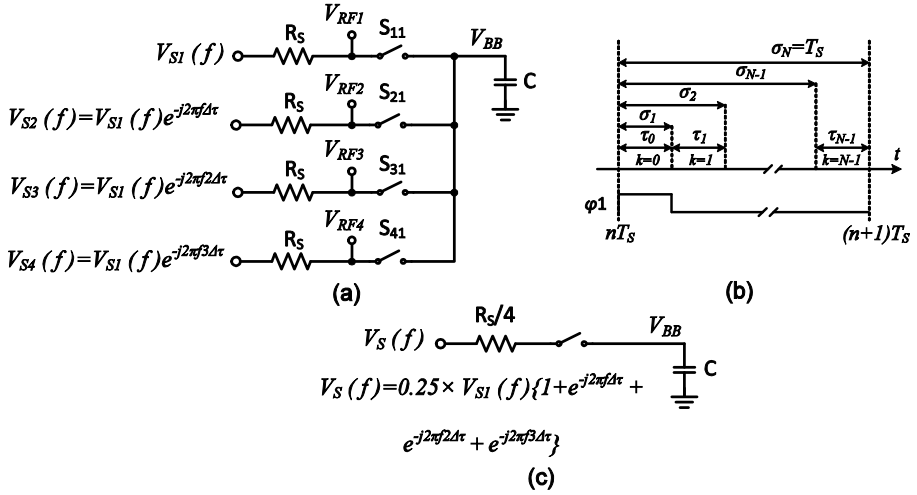

Figure 4.4. (a) Single-path of a 4-element phased-array receiver (b) Time intervals for the state-space analysis. (c) Simplified diagram for zero angle reception.

The timing diagram which is applied for the state-space analysis is shown in Fig. 4.4b. The time interval of $nT_S < t < (n+1)T_S$ is divided into N portions. At each time interval which can be shown as $nT_S + \sigma_k < t < nT_S + \sigma_{k+1}$, with $\sigma_0 = 0$, only one of "N" switches in the passive mixers is conducting. Similar to (4.2) the voltage signals V_{S1}, V_{S2}, V_{S3} and V_{S4}, are time delayed versions of the same signals for every spatial angle of "θ". From Fourier Transform theory we know that time delay causes an added linear phase in the frequency domain as: $v(t-t_d) \Leftrightarrow V(f)e^{-j2\pi ft_d}$. In Fig. 4.4a the phase shifts at different inputs are illustrated. All switches are in phase here, as the desired angle is assumed to be zero. As a result superposition can be applied and the circuit of Fig. 4.4a can be simplified to the one in Fig. 4.4c. Consequently the circuit in Fig. 4.4c can be analyzed with the LPTV approach presented in [13, 16], with two changes: 1) R_S is 4 times lower (more bandwidth); 2) the source signal contains a weighted sum of 4 antenna signals components with time shifts $(m-1)\Delta\tau$. The LPTV state-space analysis of the voltage on the baseband capacitor which is switched to the inputs at the state "k" presents a spectrum as:

$$V_{BB,k}(f,\theta) = \sum_{n=-\infty}^{\infty} H_{n,k}(f,\theta)V_{S1}(f-nf_S). \tag{4.5}$$

In (4.5) frequency shifted versions of the input spectrum are summed after weighting them by a frequency and incident angle dependent factor $H_{n,k}(f,\theta)$. The weighting factor $H_{n,k}(f,\theta)$ defined by the periodic integrating mode in which the switches are conducting and the input signals are integrated on the capacitors, followed by a hold mode in which the switches are open and the voltage on the capacitor is kept unchanged. These two modes do not have overlap in the time domain and as a result the spectrum generated by each one can be derived separately and then added up. The state-space equations for integration and hold mode are as following: $\dot{v}_{BB,k}(t) = A_k v_{BB,k} + B_k v_S(t)$ in which for the integration mode $A_{k,i} = -1/(RC)$, $B_{k,i} = 1/(RC)$, $R = R_S/4$ (index "i" stands for integration). For the hold mode the differential equation becomes as: $\dot{v}_{BB,k,h}(t) = 0$ and $A_{k,h} = B_{k,h} = 0$. The transfer function $H_{n,k}(f,\theta)$ for the baseband capacitor which is connected to the input voltage of $V_S(f)$ at time interval "k" can be found as [16]:

$$H_{n,k}(f,\theta) = \left(j2\pi fI - A_k\right)^{-1} \times \begin{pmatrix} B_k \dfrac{1-e^{-j2\pi n f_s \tau_k}}{j2\pi n} e^{-j2\pi n f_s \sigma_k} + f_s G_k(f - nf_s,\theta) e^{-j2\pi n f_s \sigma_k} \\ - f_s G_{k+1}(f - nf_s,\theta) e^{-j2\pi n f_s \sigma_{k+1}} \end{pmatrix}, \tag{4.6}$$

where the first term in the brackets is presenting the spectrum generated by the input signal when connected to the capacitor, while $G_k(f,\theta)$ and $G_{k+1}(f,\theta)$ in the second and third terms inside the brackets are illustrating the initial and end conditions on the capacitors which are added and subtracted at the beginning and end time of each time interval. The transfer function of $H_{n,k}(f,\theta)$ should encompass both the integration and hold mode. For the circuit in Fig. 4.4 the transfer function in (4.6) can be derived as: $H_{n,k}(f,\theta) = H_{n,k,i}(f,\theta) + H_{n,k,h}(f,\theta)$.

$$H_{n,k,i}(f,\theta)=\frac{e^{-j2\pi nf_s\sigma_k}}{1+j\dfrac{f}{f_{rc}}}\times\Psi\times$$

$$\left(\frac{1-e^{-j2\pi nf_s\tau_k}}{j2\pi n}+\frac{1-e^{j2\pi\left((f-nf_s)(T_s-\tau_k)-nf_s\tau_k\right)}}{2\pi\dfrac{f_{rc}}{f_s}}G_k(f)\right),$$

$$H_{n,k,h}(f,\theta)=e^{-j2\pi nf_s\sigma_k}\times\Psi\times\left(\frac{1-e^{-j2\pi f(T_s-\tau_k)}}{j2\pi\dfrac{f}{f_s}}\times e^{j2\pi\left((f-nf_s)(T_s-\tau_k)-nf_s\tau_k\right)}G_k(f)\right),$$

$$\Psi=0.25\times\left(1+e^{-j2\pi(f-nf_s)\Delta\tau}+e^{-j2\pi(f-nf_s)2\Delta\tau}+e^{-j2\pi(f-nf_s)3\Delta\tau}\right),$$

$$G_k(f)=\frac{e^{j2\pi(f-nf_s)\tau_k}-e^{-2\pi f_{rc}\tau_k}}{e^{j2\pi\frac{f-nf_s}{f_s}}-e^{-2\pi f_{rc}\tau_k}}\times\frac{1}{1+j\dfrac{f-nf_s}{f_{rc}}},\tag{4.7}$$

where $f_{rc}=(2\pi RC)^{-1}$ is defined as the 3 dB bandwidth of a single low-pass filter with resistor $R=R_S/4$ and capacitor C (see Fig. 4.4c). In (4.7) "Δτ" is time delay at different antennas defined in (4.1). "Ψ" presents the summation of the phase shifted input signals at the antenna inputs. D_k is the duty-cycle of the clock driving the switches and ideally is 1/8 for the 8 phase mixer. $H_{-3,k}(f,\theta)$ which is presenting the 3rd harmonic reception transfer for zero angle spatial reception is shown as a 3D plot in Fig. 4.5. Clearly illustrating both the Spatial- and frequency-domain filtering on the baseband capacitors around the zero degree of spatial angle. In Fig. 4.6 the cross section of the 3D plot of Fig. 4.5 for θ=0° is shown which in fact is the typical RC frequency N-path filtering of the switched-RC passive mixer transfer also discussed in [16]. To show the filtering and beamforming on the baseband capacitors, the cross sections of the 3D plot of Fig 4.5 for different offset frequencies compared to $3f_s$ are shown in Fig. 4.7a for negative offset down to $-f_s$ and in Fig. 4.7b up to f_s Please note that the amplitudes are normalized to 0 dBm in Fig. 4.7.

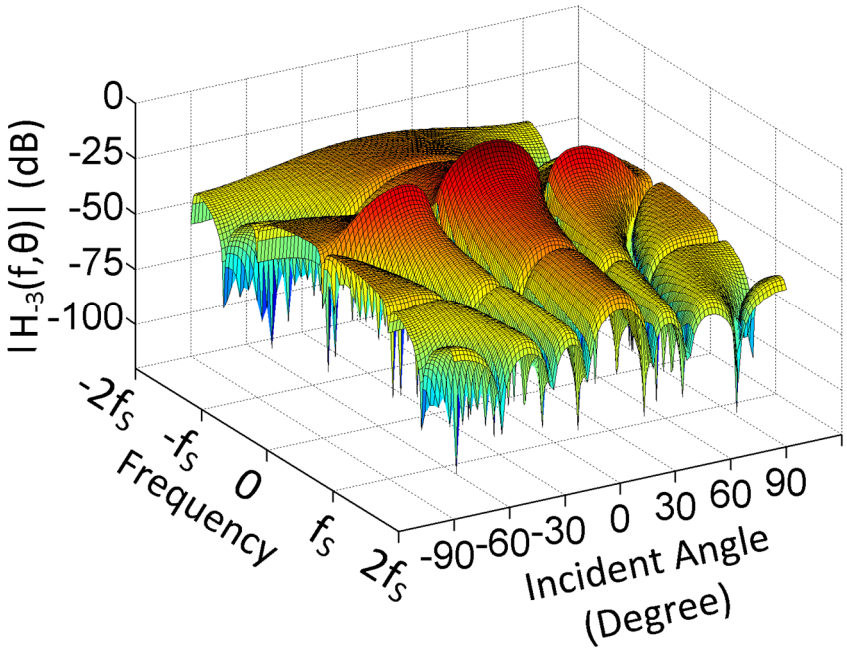

Figure 4.5. Spatial- and frequency-domain filtering on the baseband capacitors for the switching frequency f_s.

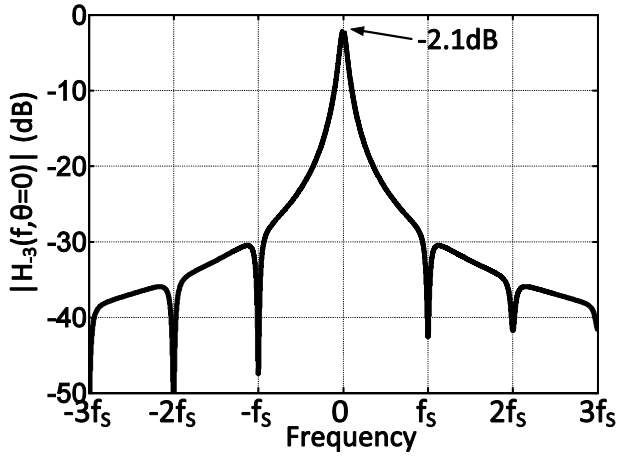

Figure 4.6. Cross section of 3D plot of Fig. 4.5 at θ=0°.

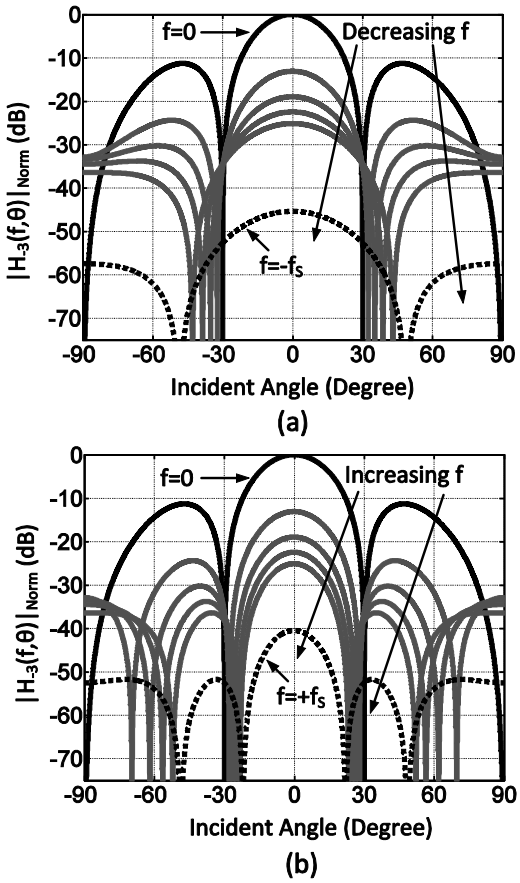

Figure 4.7. Cross section of 3D plot in Fig. 4.5 at offset frequencies.

As expected from beamforming theory positive offset frequencies (RF input frequencies higher than the 3rd harmonic) correspond to narrower beams while negative offset frequencies (RF input frequencies lower than the 3rd harmonic) correspond to wider beams. The attenuation at offset frequencies presents the frequency filtering which is also shown in Fig. 4.6 (frequency sweep).

4.4.2 Analysis at the Antenna Inputs for Zero Incident Angle

In this section mathematical derivations for the RF node at the antenna inputs are presented for the zero degree of physical angle reception. The RF node before switches in Fig. 4.4 is connected to the baseband capacitors periodically. Since there

is no overlap between switching intervals the frequency spectrum at the RF node can be derived by summing of the spectrum on all capacitors in the integration modes.

In integration mode the capacitor is connected to the RF node. As a result the integration mode equations derived for the voltage on the baseband capacitors in (4.7) can be applied:

$$V_{RF}(f) = \sum_{n=-\infty}^{\infty} H_{n,RF}(f,\theta) V_{S1}(f - nf_S),$$
$$H_{n,RF}(f,\theta) = \sum_{k=0}^{N-1} H_{n,k,i}(f,\theta), \tag{4.8}$$

where $H_{n,k,i}(f,\theta)$ is derived in (4.7). $H_{0,RF}(f,\theta)$ is defining the main transfer at the antenna inputs which is shown in Fig. 4.8. The Spatial- and frequency-domain filtering is illustrated around the 3rd harmonic of the switching frequency which is desired in our case and also around other harmonics as well. The cross section of the 3D plot in Fig. 4.8 for θ=0° is shown in Fig 4.9 which is consistent with the N-path frequency domain filtering property [13].

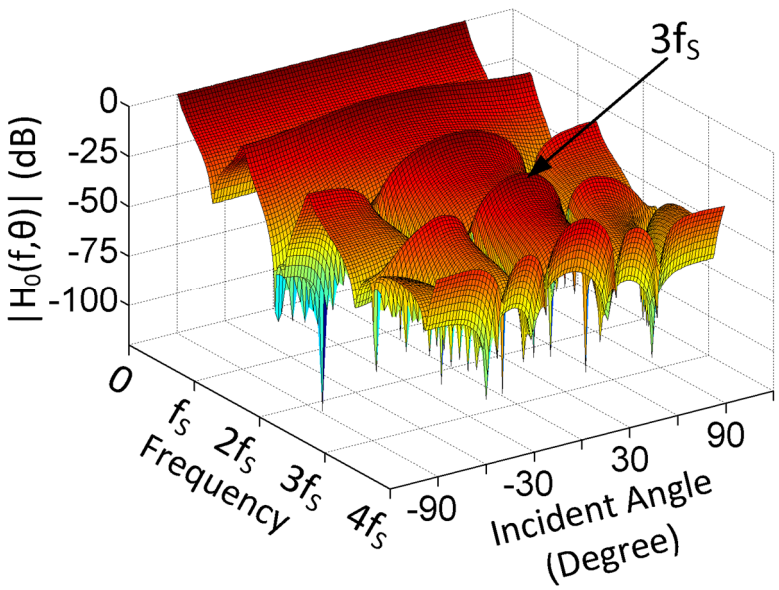

Figure 4.8. Spatial- and frequency-domain filtering at the antenna inputs for the switching frequency of f_s.

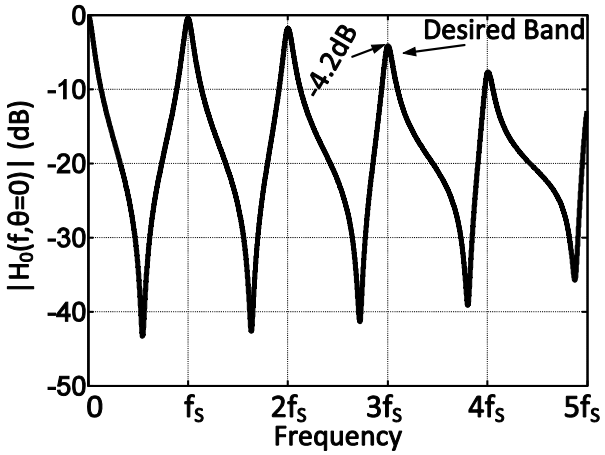

Figure 4.9. Cross section of 3D plot at θ=0° illustrating N-path frequency domain filtering at the antenna.

4.4.3 Baseband Analysis for θ=-30° of Incident Angle

Analysis of the received angle other than zero degree, requires applying a phase shift in the LO path for different antennas. As a result the switches which are connected to the same baseband capacitor will be driven with phase shifted clock signals. This is in contrast with the zero degree reception angle in which all of the switches connected to the same capacitor were in phase. Please note that 90° of electrical phase shift in the LO path will result in 270° of phase shift for the 3rd harmonic and according to (4.4) this corresponds to the spatial angle of θ=-30°. As it is shown in Fig 4.10 the incident planar wave with a spatial angle of θ=-30° at first is impinging the 4th antenna and the delayed versions of it is also hitting the other antennas. Fig 4.10 also illustrates the clocking diagram to compensate the phase shift in the LO path. Multi-phase clocks with 90° phase shifts are driving 4 switches that are connecting 4 antennas to the same capacitor. The signal which has the maximum time delay in the spatial domain, experiences minimum phase shift in the electrical domain. The LPTV analysis can be carried out again for this case to find the parameters in (4.6). The initial and end transfer functions $G(f)$ in (4.6) for each time interval can be found as following:

$$G_0 = \frac{L}{e^{\left(j2\pi\frac{f-nf_s}{f_s}\right)} - e^{\left(-8\pi D\frac{f_{rc}}{f_s}\right)}}\left\{e^{\left(-6\pi D\frac{f_{rc}}{f_s}+j2\pi(f-nf_s)(3\Delta\tau)\right)} + e^{\left(-4\pi D\frac{f_{rc}}{f_s}+j2\pi(f-nf_s)(\sigma_2+2\Delta\tau)\right)} + e^{\left(-2\pi D\frac{f_{rc}}{f_s}+j2\pi(f-nf_s)(\sigma_4+\Delta\tau)\right)} + e^{j2\pi(f-nf_s)(\sigma_6)}\right\},$$

$$G_1 = e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}.G_0 + L.e^{\left(j2\pi(f-nf_s)(3\Delta\tau)\right)},$$

$$G_3 = e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}.G_1 + L.e^{\left(j2\pi(f-nf_s)(\sigma_2+2\Delta\tau)\right)},$$

$$G_5 = e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}.G_3 + L.e^{\left(j2\pi(f-nf_s)(\sigma_4+\Delta\tau)\right)},$$

$$G_7 = e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}.G_5 + L.e^{\left(j2\pi(f-nf_s)(\sigma_6)\right)},$$

$$L = \frac{e^{\left(j2\pi D\frac{(f-nf_s)}{f_s}\right)} - e^{\left(-2\pi D\frac{f_{rc}}{f_s}\right)}}{1+j\frac{f-nf_s}{f_{rc}}}. \qquad (4.9)$$

For the hold mode the initial transfer functions will be the end condition of the previous state. Thus: $G_2 = G_1$, $G_4 = G_3$, $G_6 = G_5$, $G_8 = G_7$. With the application of (4.9) and (4.6) the voltage transfer on the baseband capacitors for the incident angle of θ=-30° can be found. The 3D plot of the result is illustrated in Fig. 4.11 in which the reception at θ=-30° for the 3rd side band and the Spatial- and frequency-domain filtering is visible.

4.4.4 Analysis at the Antenna Inputs for θ=-30° of Incident Angle

Similar to the analysis for zero angle reception in section 4.4.2 here by the superposition of the frequency spectrum on the baseband capacitors in the integration mode as in (4.8) the analysis at RF node (antenna inputs) can be found for the spatial angle reception of θ=-30°. The 3D plot for this case is shown in Fig 4.12. Again as it is expected the main beam around the 3rd harmonic of the switching frequency experience both frequency and spatial-domain filtering. The cross section of this 3D plot at θ=-30° is shown in Fig. 4.13.

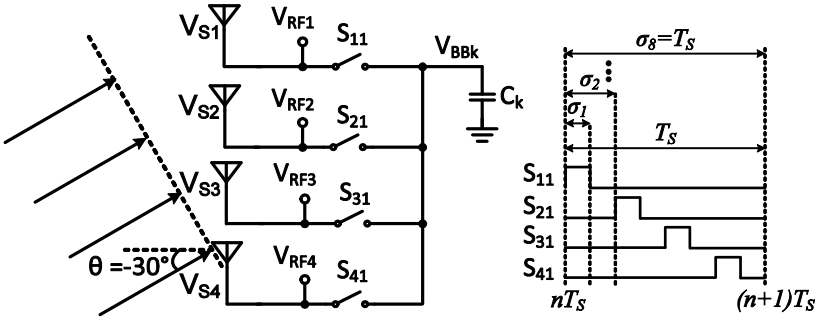

Figure 4.10. Circuit and timing diagram of reception at θ=-30°.

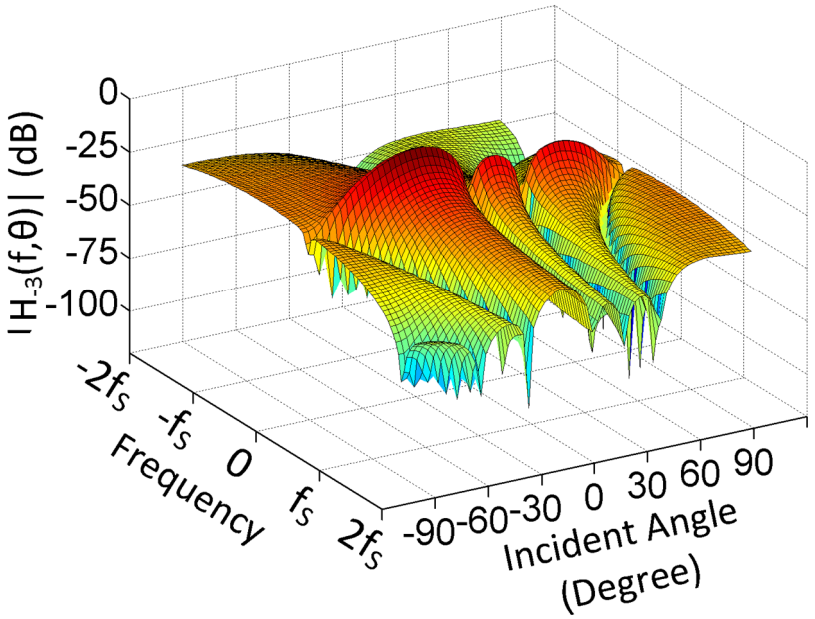

Figure 4.11. Baseband transfer of 3rd harmonic reception for the main beam at θ=-30°.

Comparing to Fig. 4.9 the harmonics other than the 3rd harmonic experience attenuation. The amount of harmonic suppression will affect the folding back from undesired harmonics with the same amount. To evaluate the amount of suppression,

contour plots derived for the 3D plot of Fig. 4.12 are shown in Fig. 4.14. Beam squinting at the offset frequencies from the 3rd harmonic is also observed.

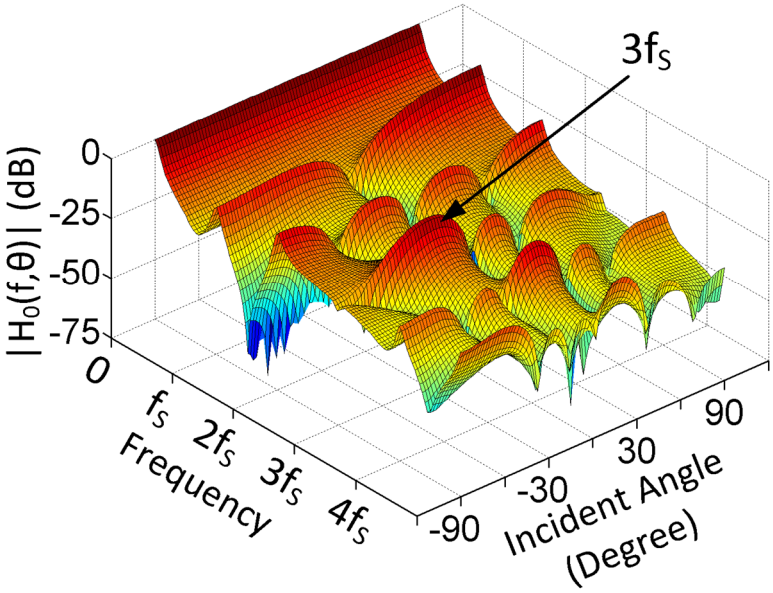

Figure 4.12. Magnitude of RF transfer at the antenna input for the main beam reception at θ=-30°.

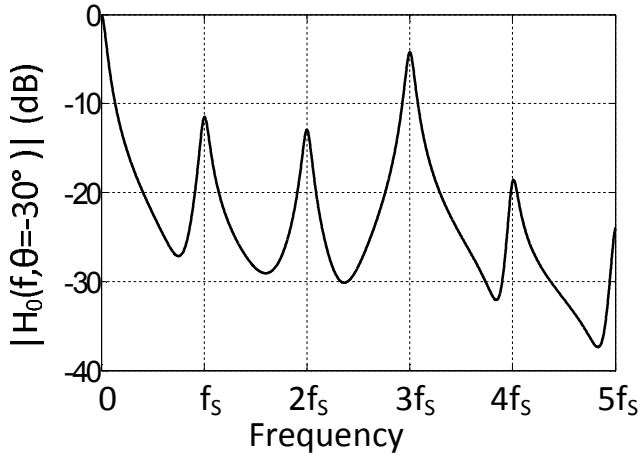

Figure 4.13. Cross section of 3D plot of Fig. 4.12 at θ=-30°.

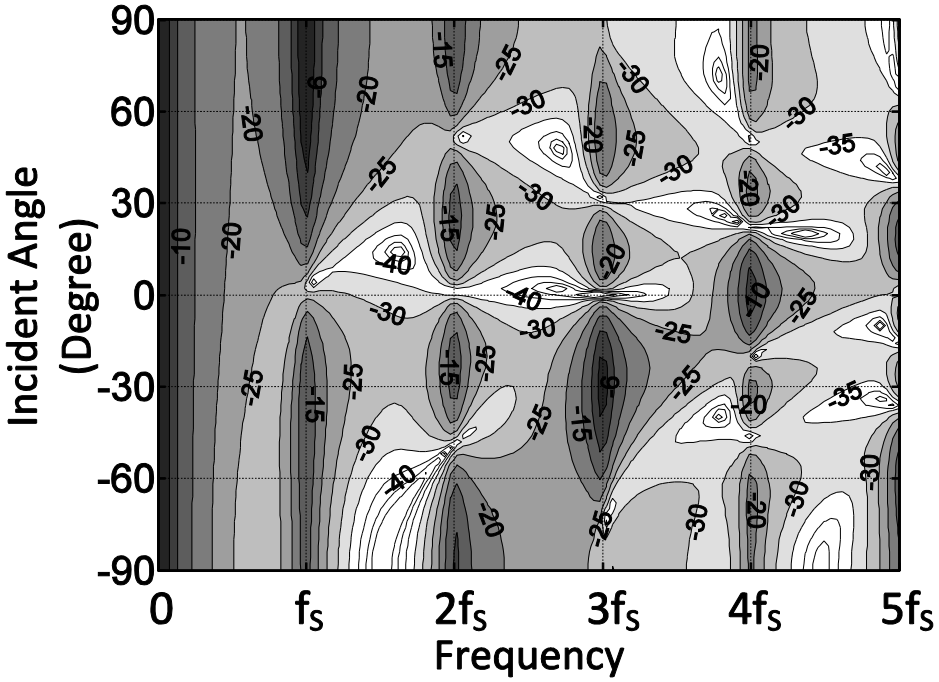

Figure 4.14. Contour plots of 3D plot of Fig. 4.12.

4.5 Implemented Architecture

The complete block diagram of the implemented prototype in 65nm CMOS technology is shown in Fig. 4.15 (see chip micrograph in Fig. 4.16). The phased-array system is composed of 4-element mixer-first architecture with 8-phase passive mixers. The mixer switches are realized with NMOS transistors (100um/0.065um) driven by 1/8 duty-cycle non-overlapped clock signals. As discussed earlier the aim is to receive the RF signals around the 3rd harmonic of the switching frequency of the passive mixers. The 8 multiphase baseband voltage signals on the capacitors are converted to the current signals via V-to-I converters (G_m blocks). The V-to-I converters are realized with self-biased inverters which can tolerate high input swings with capacitive input impedance. By proper weighting of the G_m blocks the first harmonic is rejected and the third one is received. The procedure of the vector weighting and summation is illustrated in Fig. 4.17 (note that a delay of 1/8 clock-period renders α at f_s , but 3α at $3f_s$).

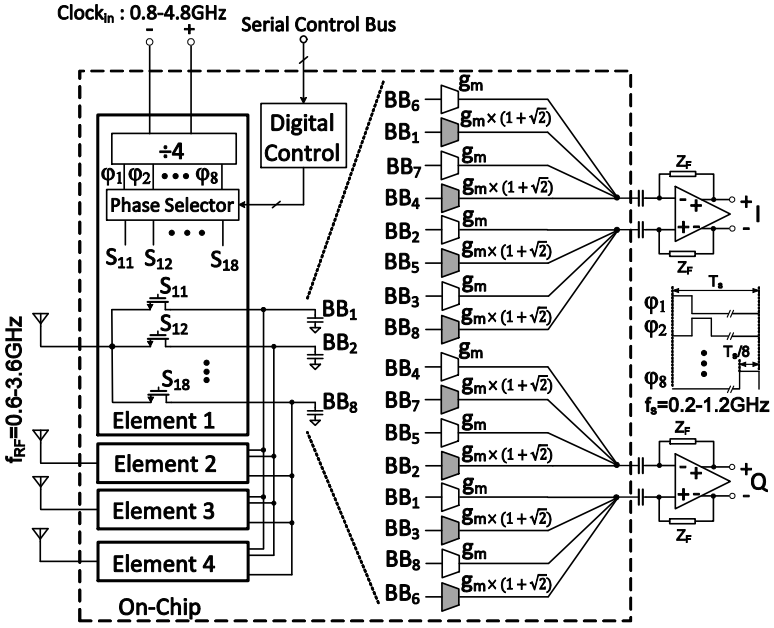

Figure 4.15. Block Diagram of the 4-element phased-array system.

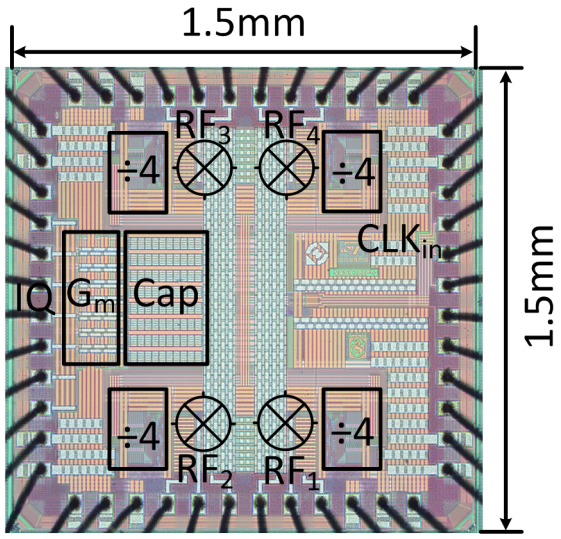

Figure 4.16. Chip micrograph in 65nm CMOS technology.

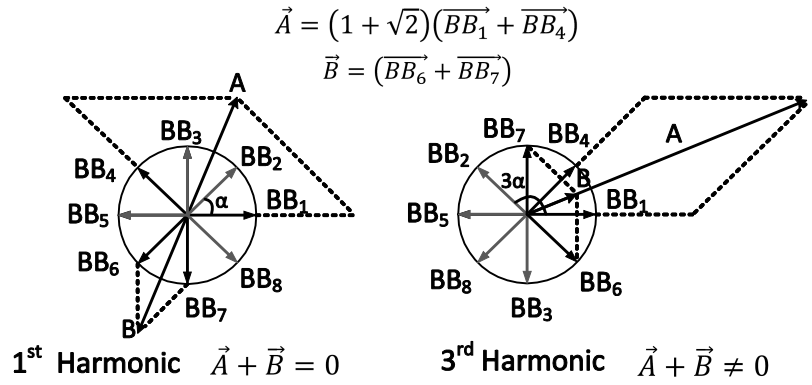

Figure 4.17. Phase summation for receiving the 3rd harmonic and rejecting 1st harmonic.

Fig. 4.17 shows how four phases of (BB1, BB4, BB6, BB7) with a proper weighting add-up constructively at the third harmonic, while they cancel each other for the first harmonic. Similarly the baseband phase summation is repeated for all other phases to generate differential IQ current signals which are combined at the output of the external Trans-Impedance Amplifiers (TIA's). The external TIA's are applied for experimental freedom and to be sure we characterize the RF front-end limitations. Since the vector summation at the output of the G_m blocks is in the current domain, a TIA can provide a virtual ground limiting the output voltage swing of the G_m blocks, which improves linearity. The clock divider architecture is illustrated in Fig. 4.18 in which a 4-stage Johnson Counter is applied. Since we have applied single-ended mixers, the flicker noise of the clock divider core might easily leak to the baseband outputs. In order to avoid this we have applied a re-clocking scheme. The output phases of the divider are combined by 4-input NAND gates (two pairs of complementary inputs) to generate ¼ duty-cycle clocks enable signals. Depending on the output, either master clock CB or CA do the re-clocking, generating a 1/8 duty-cycle at the output (see Fig. 4.18). In the clock divider core, the Johnson divider and the phase combining part are now allowed to have high noise. Only the re-clocking path at the output of transmission gates requires clean clock edges of the master clock. The phase selector in Fig. 4.15 with a digital control unit which is controlled externally via a serial bus provides full programmability of clock phases driving the mixer switches. This is required to rotate the beam to different angles.

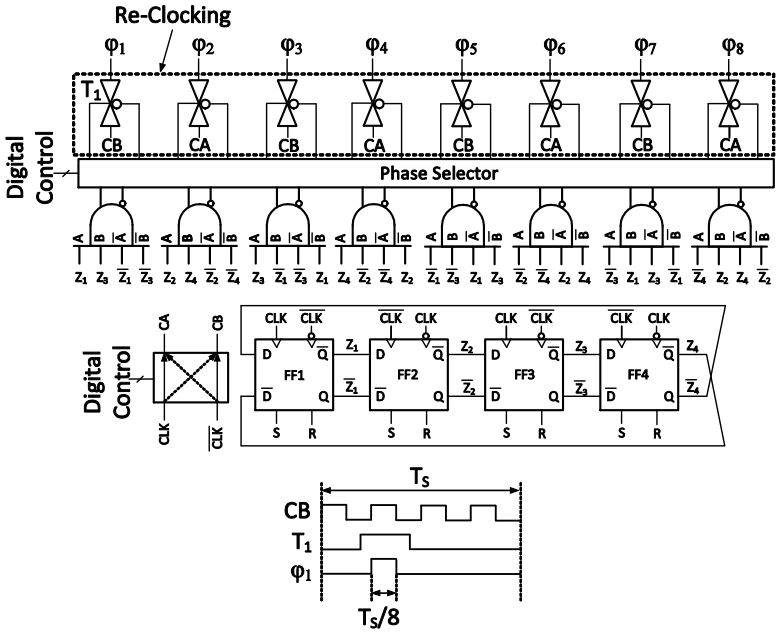

Figure 4.18. Block diagram of the clock divider.

4.6 Analysis Implications

In this section the analysis results in section 4.4 are applied for the architecture described in section 4.5, to discuss the conversion-gain, input power matching and noise behavior of the receiver architecture illustrated in Fig. 4.15. As we assumed in the analysis section for simplicity purposes the switches are assumed to be ideal (zero "ON" resistance and infinite "OFF" resistance).

4.6.1 Conversion Gain

The mixer conversion gain on the baseband capacitors for the 3rd harmonic reception in a single-element can be found from $H_{n,k}(f,\theta)$ defined in the general form in (4.5). $H_{n,k}(f,\theta)$ is derived for the desired angle of θ=0° in (4.7). Substituting n=±3, θ=0°, f=0 for the 3rd harmonic reception, we find mixer conversion-gain as: $CG_{M3} = H_{n=\pm 3,k}(f=0,\theta=0°) \approx -2.1dB$ or 0.78V/V in linear scale which is also shown in Fig. 4.6. This is compared to

the first harmonic reception which again can be found from (4.7) as $CG_{M1} = H_{n=\pm1,k}(f=0,\theta=0°) \approx -0.2dB$. As we will see in section 4.6.3 this difference in the conversion gain of the first and the 3rd harmonic reception, as it is expected will translate to about 2 dB degradation in the noise figure for 3rd harmonic reception compared to the 1st harmonic.

In order to find the total conversion-gain to the I/Q output in Fig. 4.15, considering the phase diagram in Fig. 4.17, we find the differential output voltage transfer $H_{n,I}(f,\theta)$ for "I" output as:

$$H_{n,I}(f,\theta) = 2Z_F g_m \left\{(1+\sqrt{2})\left(H_{n,1}(f,\theta)+H_{n,4}(f,\theta)\right)+ \left(H_{n,6}(f,\theta)+H_{n,7}(f,\theta)\right)\right\}, \tag{4.10}$$

where $H_{n,k}(f,\theta)$ for k=1,4,6,7 is defined in (4.5). As an example for zero angle reception, the receiver conversion-gain for 3rd harmonic reception (voltage transfer from TIA-output "I" to the single-ended input) is found as:

$$CG_{R3} = \frac{V_{out,I}}{V_s} = H_{n=\pm3,I}(f=0,\theta=0°) \approx 8.2 \times Z_F g_m . \tag{4.11}$$

Please note that, in case of receiving the frequency band around the first harmonic of the switching frequency instead of the 3rd harmonic, the voltage conversion-gain will be about 2 dB larger than the value in (4.11).

4.6.2 Input Power Matching

In order to find the conditions to provide input power matching around the third harmonic of the switching frequency, the transfers for the RF node before switches in Fig. 4.15 should be applied. For this purpose (4.8) is approximated around the harmonics of the switching frequency with the assumption of: $f_s >> f_{rc}$, $f \approx nf_s$ and "n" is an integer number. This approximation for the zero angle reception becomes as the following:

$$H_{0,RF}(nf_S,\theta=0) \approx \frac{2N(1-\cos(2\pi nD))}{4D(n\pi)^2} + (1-ND) \qquad 0 < D \le 1/N. \tag{4.12}$$

Assuming N=8, n=3, D=1/8 we find $H_{0,RF}(3f_s,\theta=0)\approx 0.62V/V$ which translates to the input impedance of $Z_{in}(3f_s,\theta=0)\approx 1.6R_S$. This value for input impedance does not provide power matching with the source impedance of R_S. However; the parasitic capacitance of the switches at the antenna side reduces the input impedance to a value which is close enough to 50 Ω for reasonable matching.

4.6.3 Noise Analysis

In this section we are aiming to provide an insight to the noise behavior of the phased-array receiver architecture presented in Fig. 4.15. In this regard we assume that the noise is dominated with the mixer at the input. This means the noise of G_m blocks and TIAs is negligible. In order to find the total noise power at the output, the transfer function derived in (4.10) can be applied. As a result the total noise transfer at the "I" output can be derived as:

$$N_{out,I}=\left(\sum_{n=-\infty}^{\infty}\left|H_{n,I}(f,\theta)\right|^2\right)N_{in}\,|_{f=0,\theta=0^\circ}\approx 218.4\times(Z_F g_m)^2 N_{in}, \tag{4.13}$$

in which $H_{n,I}(f,\theta)$ is defined in (4.10) and finally the Single-Side-Band (SSB) noise figure for the single-element receiver and 3rd harmonic reception, can be found as:

$$NF_{SSB,3}=10\log\left(\frac{N_{out,I}}{CG_{R3}^2\times N_{in}}\right), \tag{4.14}$$

in which CG_{R3} is defined in (4.11). Evaluating (4.14) gives $NF_I\approx 5dB$. Considering image rejection, the double side band noise figure is 3 dB lower than this value. In a practical implementation the switch resistance will add noise to the circuit; moreover the non-ideal clocking will reduce the conversion gain resulting in increased noise. Noise from G_m blocks will add-up to the noise calculation in this section as well.

In case we applied 1st harmonic reception the output noise calculated in (4.13) will not change, while the conversion gain will be increased by about 2 dB, which will translate to the NF improvement with the same amount.

4.7 Measurements

An external clock with a frequency range of 0.8-4.8GHz is divided by 4 on-chip, providing the 3rd harmonic reception of 0.6-3.6GHz (ratio 3/4). In order to measure beam patterns, 4 RF signal generators with a variable well-controlled phase difference are applied to emulate the incident signals impinging the receiver antennas from different spatial directions.

The constructed beam pattern for broadside reception at 2.4GHz ($f_s = 800MHz$) is shown in Fig. 4.19 (equal phase settings). It largely follows the ideally switched 4-element phased-array (gray line). In order to illustrate the spatial filtering at the antenna inputs, the compression point (P_{1dB}) of 4-elements is measured versus the incident angle of the blocking signal. The output power level of the 4 RF signal generators (with proper phase difference) are swept and the compression point was measured, observing the IF signals (see Fig. 4.19). While the measured results show a P_{1dB}=-5.5 dBm for zero incident angle, it increases to up to +10 dBm at null points, i.e. up to more than 15 dB spatial rejection. The maximum improvement is limited due to the effect of the switch resistance.

In Fig. 4.20 also the constructed beam patterns for 8 uniformly spaced electrical phase shifts are presented as polar plots. As discussed in section 4.3.2, a maximum gain is achieved for the spatial angles 0, ±14.48, ±30, ±48.6 and 90 degrees, corresponding to electrical LO phase shifts of (0, ±45, ±90, ±135, 180 degrees) and antenna physical distance of d=λ/2 where λ is the wavelength of the incident RF signal. The beam patterns are superimposed in a single figure in Fig. 4.21, showing a maximum gain variation of 0.8 dB over different directions.

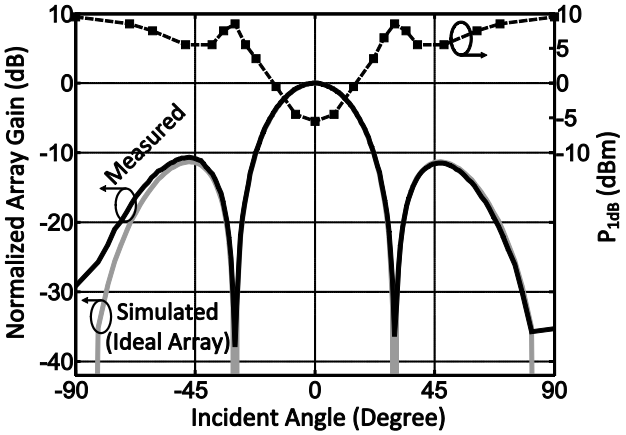

Figure 4.19. Beam pattern at zero incident angle and P_{1dB} measurements at f=2.4GHz received band.

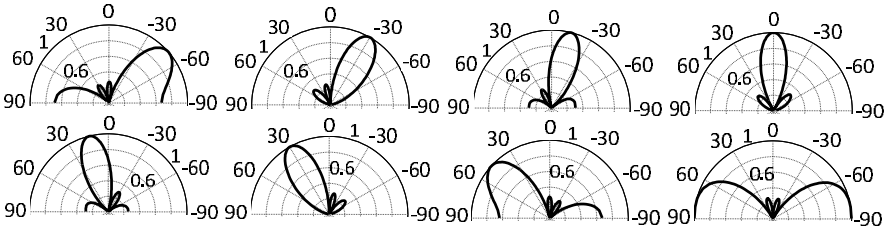

Figure 4.20. Constructed beam patterns at f=2.4GHz received band.

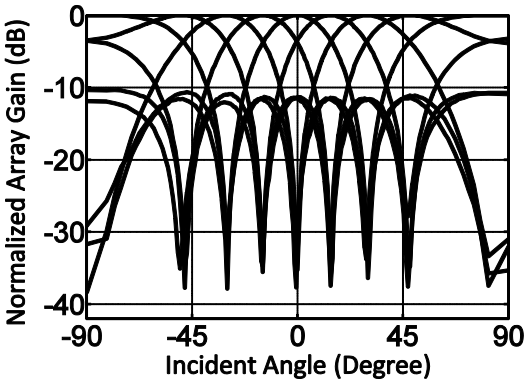

Figure 4.21. Constructed beam patterns at f=2.4GHz received band.

The IF transfer curves for 1-element and 4-elements are shown in Fig. 4.22. The measured 3 dB bandwidth for the single element is 5MHz (10MHz @ RF). In this measurement the external TIAs were replaced by 10 Ω differential resistors in order to eliminate TIA bandwidth limitations. When all 4 elements are activated, the effective resistance seen by the capacitors "looking to the antennas" is reduced by a factor of 4 resulting in 4 times larger bandwidth. As shown in Fig. 4.22 P_{1dB} increases to up to +11 dBm for out of band blockers with 4-elements. Fig. 4.23 shows the single element DSB NF of 3-6 dB. Please note that the calculated noise figure of a simplified model in section 4.6 resulted in 2 dB DSB NF. Neglecting the shared noise in the 4 paths generated by G_m blocks, 6 dB improvement in SNR is expected. However, noise floor measurements at the output show 4 dB instead of 6 dB, due to the shared noise of G_m blocks. Simulations show 4.5 dB improvement in NF. All analog G_m blocks consume 36mW together providing 100mS in each of the I and Q paths.

Overall power consumption with 4 elements activated is 68-195mW for the received frequency range of 0.6-3.6GHz. The maximum ripple in the gain is 2.5 dB and in-beam/band IIP3 varies from +2.. +9 dBm (see Fig. 4.23). The measured S_{11} is shown for three switching frequencies in Fig. 4.24, consistently giving better than -10 dB of S_{11} in the received band. S_{11} is measured with just one element and also with 2 elements activated, where the latter (common mode) S_{11} shows a broader dip in Fig. 4.24, consistent with doubled bandwidth as discussed earlier. This measurement proves that indeed filtering takes place at the antenna inputs. The LO leakage to RF nodes at the antenna inputs is measured from -69 to -60 dBm at 3rd harmonic for the received frequency range of 0.6-3.6GHz. The first harmonic is rejected between 15-25 dB. The measurement results are compared to three previously reported 4-element phased-array systems. Clearly remarkable P_{1dB} and NF are achieved, and the dynamic range at the antenna inputs is substantially improved compared to previous work.

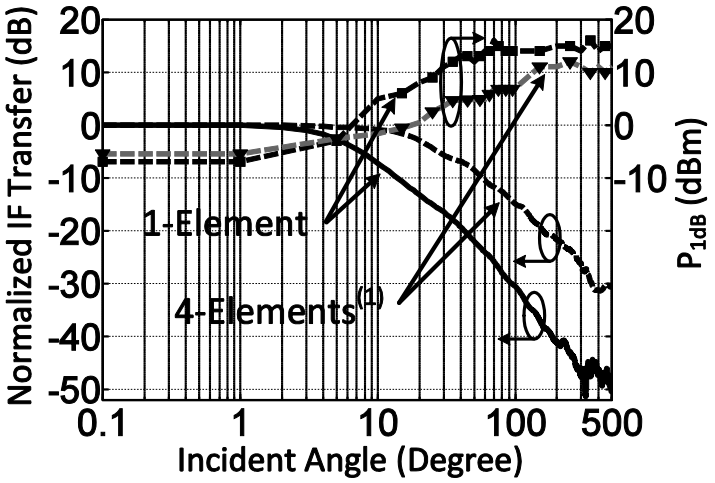

Figure 4.22. IF transfer and P_{1dB} at f=2.4GHz RF frequency.

(1) P_{1dB} is measured with 4-elements, but power is referred to the single-element input.

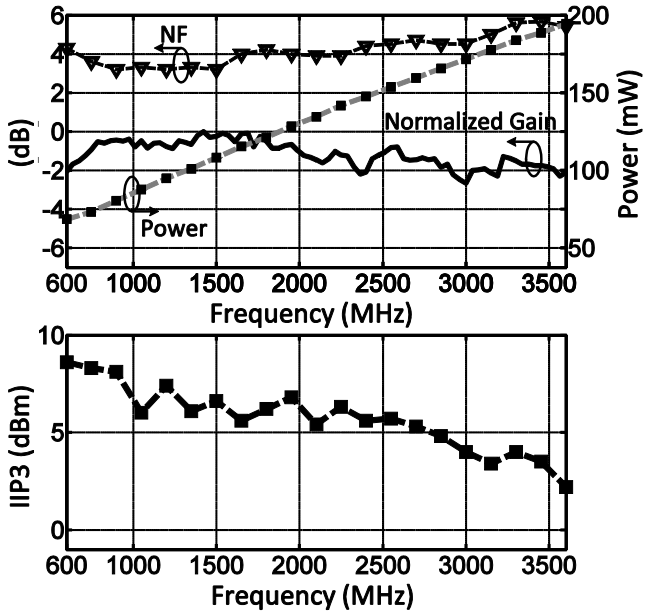

Figure 4.23. NF, normalized gain and in-beam/band IIP3 of single-element, and power consumption of 4 elements versus received frequency.

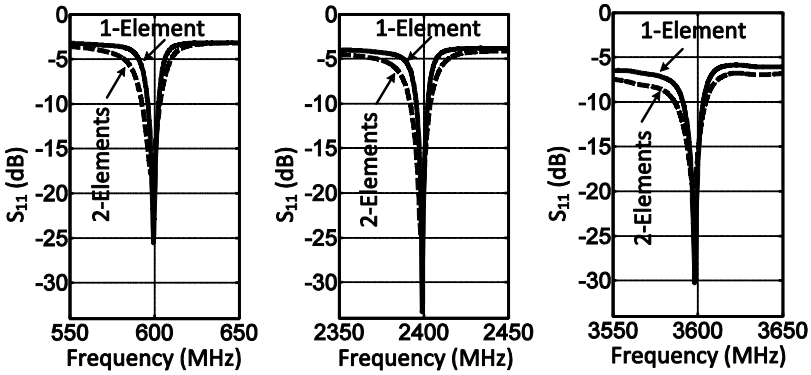

Figure 4.24. Measured S_{11} for 1-element and 2-elements activated at three received frequencies bands.

Table 4.1. Comparison of CMOS 4-element phased-array systems.

	[4]	[5]	[6]	This Work
Technology	CMOS 90nm	CMOS 65nm	CMOS 65nm	CMOS 65nm
Active Die Area (mm^2)	1.4	0.44	0.18	0.97
RF Frequency (GHz)	4	1-4	1.5-5	0.6-3.6
Phase/Amplitude Resolution (bits)	5 / 3	5 / 3	5 / -	3 / -
4-Elements Power (mW)	166	308	65-168	68-195
1-Element IF Bandwidth (MHz)	NA	65	300	5[(1)]
1-Element Noise Figure (dB)	13	10	18	3-6
4-Elements SNR Improvement (dB)	6[(2)]	6[(2)]	6[(2)]	4
1-Element Input Referred P_{1dB} (dBm)	NA	-14	2	-5.5 (In-Beam/Band)[(3)] +10 (Out-of-Beam)[(3)] +11 (Out-of-Band)[(3)]
1-Element IIP3 (dBm)	2	-1	13	+2 .. +9 (In-Beam/Band)[(3)]

[(1)] IF_{BW}=20MHz when 4 elements are activated (see Fig. 4.4).
[(2)] 6 dB improvement in SNR is expected but not measured.
[(3)] Measured with 4-elements, but power is referred to the single-element input.

4.8 Conclusions

Both Spatial- and frequency-domain filtering is presented directly at the antenna inputs by a 4-element phased-array receiver. By applying passive mixers directly at the antenna and summation of the multiphase signals directly at the baseband capacitors, an angle dependent P_{1dB} is achieved with an improvement of up to 15 dB for out-of-beam/band signals. Hard-driven switches implementing passive mixers provide high linearity of up to +9 dBm. By exploiting 3rd harmonic downmixing, high RF frequencies up to 3.6GHz are covered at relatively low power. A large tuning range of 0.6-3.6GHz with simultaneous Spatial- and frequency domain filtering can be useful for in- and out-of-band blocker rejection and for future dynamic spectrum access applications exploiting software-defined or cognitive radio.

4.9 References

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Chapter 5

Conclusions

5.1 Summary and Conclusions

A brief introduction on tunable RF filtering requirements for DSA applications is presented in chapter 1. It is motivated that the availability of tunable on-chip filters would decrease the cost and size of the multi-mode multi-band wireless transceivers. Moreover for the upcoming generation of cognitive wireless communication systems, the received frequency band would vary over time and location, and tunable RF filtering is a critical bottleneck. The currently commonly used SAW/BAW filter technology can provide good filter shape, but has very limited tuning capabilities. CMOS compatible approaches are very much wanted and are explored in this thesis. Switched RC N-path filters based on MOS switches and capacitors look promising as switches and capacitors can be implemented attractively in downscaled CMOS processes.

In chapter 2 a differential single-port switched-RC N-path filter with a band-pass characteristic is discussed. As it is shown the switching frequency defines the center frequency, while the RC-time and duty-cycle of the clock define the bandwidth.

This allows for high-Q highly tunable filters which can for instance be useful for cognitive radio. Using a linear periodically time-variant (LPTV) model, exact expressions for the filter transfer function are derived. By applying the mathematical results the behavior of the circuit including non-idealities such as maximum rejection, spectral aliasing, noise and effects due to mismatch in the paths are modeled and verified via measurements. A simple RLC equivalent circuit is provided, modeling bandwidth, quality factor and insertion loss of the filter. As we discussed in chapter 2, a 4-path architecture is realized in 65 nm CMOS. In measurement setup an off-chip transformer which acts as a balun, improves filter-Q and realizes impedance matching. The differential architecture reduces clock-leakage and suppresses selectivity around even harmonics of the clock. The bandpass filter has a constant -3 dB bandwidth of 35 MHz and can be tuned from 100 MHz up to 1 GHz. Over the whole band, IIP3 is better than 14 dBm, P_{1dB}=2 dBm and NF is 3-5 dB, while the power dissipation increases from 2 mW to 16 mW (only clocking power).

Bandstop or notch filters can alleviate the coexistence problem in multi-mode multi-standard wireless communications. Tunable notch filtering is also highly wanted in dynamic spectrum access applications to suppress unwanted blocking signals which can vary over different frequency bands. In chapter 3, N-path notch filters are discussed. Similar to the N-path bandpass filters, both differential and single-ended N-path notch filters are modeled and analyzed where closed-form equations provide design equations for the main filtering characteristics and non-idealities such as harmonic mixing, switch resistance, mismatch and phase imbalance, clock rise and fall times, noise and insertion loss. Both an 8-path single-ended and differential notch filter are implemented in 65 nm CMOS technology. The notch center frequency which is determined by the switching frequency is tunable from 0.1-1.2 GHz. In a 50 Ω environment the N-path filters provide power matching in the pass-band with an insertion loss of 1.4-2.8 dB. The rejection at the notch frequency is 21-24 dB, P_{1dB}> +2 dBm and IIP3> +17 dBm.

In-band blocking signals cannot be suppressed by frequency-domain filtering, while spatial-domain filtering provided by phased-array systems can be applied to suppress the in-band blockers impinging the antennas with a spatial angle different from the desired signal. The N-path filtering concept is adopted in a 4-element LO-phase shifting phased-array system in chapter 4, where a prototype with 8-phase passive mixers terminated by baseband capacitors, realized in 65 nm CMOS. The passive mixers upconvert both the spatial and frequency domain filtering to RF, realizing blocker suppression directly at the antenna inputs. Utilization of 3rd

harmonic reception widens the frequency range to 0.6-3.6 GHz at 68-195 mW power dissipation. The implemented phased-array system presents high linearity and compression point with a rather reasonable noise figure. Up to +10 dBm of P_{1dB} for out-of-beam/band, a 1-element NF of 3-6 dB and in-beam/band IIP3=+2..+9 dBm are measured.

The N-path filtering blocks discussed in this theses provide inductorless high-Q, tunable bandpass and bandstop filters with high linearity and compression point at RF frequencies. They benefit from CMOS scaling and might be applicable in the context of upcoming dynamic spectrum access applications to implement low-cost, compact and reconfigurable wireless transceivers.

5.2 Original Contributions

1. Implementation of a differential 4-path switched RC bandpass filter for RF pre-filtering.
2. The mathematical analysis of switched RC N-path bandpass filters including the filtering behavior and effects of the imperfections on the filter performance.
3. The design and implementation of 8-path switched RC single-ended and differential bandstop (notch) filters.
4. The mathematical analysis of the functional properties and imperfections of the N-path notch filters.
5. The design and implementation of a 4-element mixer first phased-array system providing simultaneous spatial and frequency-domain filtering at the antenna inputs accompanied by the mathematical modeling

5.3 Future Work

With the availability of highly linear switches and high density capacitors in the new CMOS technologies, the application of switching circuits is becoming increasingly attractive in wireless transceiver architectures. In this regard passive switching mixers with RC networks in the form of N-path filters have strong potential to be explored and utilized as an inductorless high-Q filtering approach. This technique provides high linearity, high compression point, low noise as well as flexible digital tunability, which are all interesting properties for the DSA applications. We have explored the switched-RC filtering behavior and its applications at RF frequencies.

A single N-path network as discussed in this thesis still has substantial limitations which can be addressed. Some suggestions for future work directions are given below.

1. The harmonic mixing of the passive hard switching mixers causes systematic harmonic folding in the N-path filters. The folded harmonics can be pushed further away by increasing the number of paths and clock phases. However, rejection is never perfect due to unavoidable component mismatches, so that residues remain. Thus a time invariant RF pre-filter is needed which is undesirable. Moreover, there is harmonic selectivity in the filtering transfer function of the N-path filters. This means apart from the selectivity around the main harmonic which is desired there is frequency selectivity around higher harmonics of the switching frequency. With the application of a differential architecture the even harmonic selectivity is suppressed; however the selectivity around odd harmonics still exist in the N-path filters discussed in this thesis. Unlike the harmonic folding the harmonic selectivity cannot be canceled by increasing the number of paths. RF pre-filtering might be an option to remove the possible interfering signals on the harmonic frequencies before these signals are delivered to the N-path filters but finding a CMOS compatible way to avoid external RF pre-filtering is preferred.

2. The phase noise on the clock applied for driving the switches in N-path filters, might cause unwanted folding from nearby blockers on top of the desired band especially for the bandpass N-path filters. Straightforward analysis results are presented in [1] where implications are drawn from the analysis indicating that N-path filters are more susceptible to common-mode noise than differential mode noise coming from the clock network. While the conceptual implications are verified via Verilog-A modeling of phase noise on the clock network the analyzed equation are not verified directly via simulation or measurements. There is a research space in this area to provide comprehensive and accurate analysis of the phase noise effect on the performance of N-path filters.

3. Another important factor which might be considered for future work is the nonlinearity effects caused by switches and capacitors. In our mathematical approach we have assumed perfectly linear switches and capacitors which is not the case in real life. Although the CMOS switches and capacitors provide very high linearity, the dominant nonlinearity factors continues to be an interesting research topic.

4. In the N-path filters which are analyzed in this thesis the source impedance in the bandpass filter and both source and load impedances in the notch filters are assumed to be purely resistive. However there might be parasitic reactive components associated with the switches or the blocks connected to the N-path filters such as antenna or RF pre-filters. Purely resistive impedance simplifies the analysis to a single state case without interaction among the voltages on different capacitors. There has been recently some efforts to address this issue [1, 2]. However, the presented approaches are based on some approximations on the out-of-band behavior of the N-path filters and are verified just for very simple one or two reactive components. A more accurate analysis approach addressing reactive components in combination with the switching elements might be a future research area.

5.4 References

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List of Abbreviations

ADC	Analog to Digital Converter
BAW	Bulk Acoustic Wave
BPF	Bandpass Filter
BSF	Bandstop Filter
BT	Bluetooth
CMOS	Complementary Metal Oxide Semiconductor
DAC	Digital to Analog Converter
DSA	Dynamic Spectrum Access
DSB	Double-Side-Band
DSP	Digital Signal Processing
FCC	Federal Communication Commission
FDD	Frequency Division Duplexing
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HPF	Highpass Filter
IIP2	Input-Referred 2^{nd} Order Intercept Point
IIP3	Input-Referred 3^{rd} Order Intercept Point
IM2	Second-Order Intermodulation
IM3	Third-Order Intermodulation
LNA	Low Noise Amplifier
LNTA	Low Noise Trans-Conductance Amplifier
LO	Local Oscillator
LPF	Lowpass Filter
LPTV	Linear Periodically Time Variant
LTI	Linear Time Invariant
MEMS	Micro-Electro-Mechanical Systems
MIM	Metal-Insulator-Metal
NF	Noise Figure
OFDM	Orthogonal Frequency-Division Multiplexing
P_{1dB}	One dB Compression Point

PA	Power Amplifier
PVT	Process Voltage Temperature
Q	Quality Factor
RF	Radio Frequency
SAW	Surface Acoustic Wave
SDR	Software-Defined Radio
SE	Single-Ended
SNR	Signal to Noise Ratio
SSB	Single-Side-Band
SWR	Software Radio
TIA	Trans-Impedance Amplifier
TVWS	TV White Spaces
UMTS	Universal Mobile Telecommunication System
VGA	Variable Gain Amplifier
WRAN	Wireless Regional Area Network

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List of Publications

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